

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

LG DISPLAY CO., LTD.,)	
)	
Plaintiff,)	Civil Action No. 06-726 (JJF)
)	Civil Action No. 07-357 (JJF)
v.)	
)	CONSOLIDATED CASES
CHI MEI OPTOELECTRONICS)	
CORPORATION, et al.)	
)	
Defendants.)	
)	
)	

**MEMORANDUM IN SUPPORT OF
DEFENDANTS CHI MEI OPTOELECTRONICS'
PROPOSED CLAIM CONSTRUCTIONS**

OF COUNSEL:

Morgan Chu
Jonathan S. Kagan
Alexander C.D. Giza
Adam Hoffman
Irell & Manella LLP
1800 Avenue of the Stars, Suite 900
Los Angeles, California 90067-4276
(310) 277-1010

Dated: August 11, 2008

Philip A. Rovner (#3215)
POTTER, ANDERSON & CORROON LLP
Hercules Plaza
1313 N. Market St.
P.O. Box 951
Wilmington, Delaware 19899-0951
(302) 984-6000
provner@potteranderson.com

*Attorneys for Defendant
Chi Mei Optoelectronics Corporation*

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I. INTRODUCTION

Chi Mei Optoelectronics Corporation and Chi Mei Optoelectronics USA (collectively, “CMO”) submit this brief in support of their proposed patent claim constructions in the above captioned cases. In total, this case involves twenty-three patents asserted by three different parties. The only claim terms addressed by this brief, however, are disputed terms in the six patents CMO has asserted against LG Display Co., Ltd. and LG Display America, Inc. (collectively, “LGD”), and the eight patents asserted by LGD against CMO.¹

Three of LGD’s patents – the ‘002, ‘449 and ‘737 patents² – have been litigated before and were the subject of claim construction rulings in prior cases in California (the “LGD/CPT I case”) and Delaware (the “LGD/CPT II case”). Exs. C-5, C-7, B-4 [Markman rulings]. LGD is now attempting to deviate from a number of these prior claim construction rulings – even ones that it proposed and prevailed on in the prior litigations. Where possible, however, CMO has attempted to adopt with the prior courts’ constructions of terms that LGD has already litigated. For these claim terms, LGD may not now re-litigate claim construction to define its patents differently against CMO.

The disputed terms and the parties’ proposed constructions are listed in the Joint Claim Construction (“JCC”) chart, which is attached as Appendix 1. The charts for each individual patent are attached to the JCC as JCC Exhibits A-I and R-W, for the LGD and CMO patents, respectively.

The patents at issue relate to various aspects of liquid crystal displays (“LCDs”). LCDs include a liquid crystal material sandwiched between a pair of supporting materials, called substrates, and a pair of light filters, called optical polarizers. The substrates support thin film transistors (“TFTs”) in a way that creates a two-dimensional grid of pixels. Every pixel, or spot,

¹ An additional patent (U.S. Patent 6,664,569) is presently asserted by LGD only against AU Optonics (“AUO”), and eight additional patents are asserted by AUO against LGD. CMO has not been involved in the claim construction process for the AUO patents or LGD’s ‘569 patent.

² In this brief, CMO is following the standard practice of identifying each patent by the last three digits of its patent number.

on the display is individually accessed by its corresponding TFT. Driver circuitry provides signal voltages to the TFTs, which apply a voltage that changes the orientation of the liquid crystal material so that light is either emitted or blocked by one of the polarizers, thus changing the intensity of the illumination of that pixel. The combination of a set of primary color pixels (typically red, green, and blue) provides the full spectrum of colors that a person sees when looking at the LCD.

In general, the '737, '449, '274, '321 and '489 patents describe and claim different processes and structures for the TFTs. The '923 and '002 patents relate to preventing electrostatic discharge from damaging the transistors during the fabrication of the LCDs. Processes for sealing the LCDs are disclosed in the '179 and '374 patents. The '984 patent involves the use of a single production line for dispensing liquid crystal material and sealant. The '092 patent describes an illumination device for guiding light to the liquid crystal layer of an LCD. The '786 patent discloses a technique for correcting the color of a LCD for differences in the amount of light transmitted (transmissivity) through the display for different colors. The '352 patent discloses an optical compensator that increases the viewing angle of an LCD. The '926 patent discloses a method of placing control circuitry within an LCD panel to minimize the thickness of the LCD device. A more detailed discussion of each patent and CMO's arguments for claim constructions are provided in each patent section of this brief.³

II. ARGUMENT

A. PRINCIPLES OF CLAIM CONSTRUCTION

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (citing *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)), *cert. denied*, 546 U.S. 1170 (2006). A patentee

³ CMO also presents expert declarations to provide background and explain the technologies of the patents in suit. Declaration of Dr. Miltiadis Hatalis ("Hatalis Decl."); Declaration of Dr. John Villasenor ("Villasenor Decl."); Declaration of Dr. Pochi Yeh ("Yeh Decl.").

must “particularly poin[t] out and distinctly clai[m] the subject matter which the applicant regards as his invention,” 35 U.S.C. § 112, ¶ 2, to satisfy the policy concern that a “patent holder should know what he owns, and the public should know what he does not.” *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722, 731 (2002). Indeed, “the patentee is required to ‘define precisely what his invention is,’” and therefore “it is ‘unjust to the public, as well as an evasion of the law, to construe it in a manner different from the plain import of its terms.’” *Phillips*, 415 F.3d at 1312 (citing *White v. Dunbar*, 119 U.S. 47, 52 (1886)).

The purpose of claim construction is to determine what the applicants claimed. Claim construction begins with the “words of the claims themselves.” *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). The “words of a claim are generally given their ordinary and customary meaning” as would be understood by “a person of ordinary skill in the art in question at the time of the invention, *i.e.*, as of the effective filing date of the patent application.” *Aquatex Indus., Inc. v. Techniche Solutions*, 419 F.3d 1374, 1380 (Fed. Cir. 2005), *further proceeding*, 479 F.3d 1320 (Fed. Cir. 2007).

Claim terms are to be read in light of the specification, *United States v. Adams*, 383 U.S. 39, 48-49 (1966), and in light of the “fundamental purpose and significance” of the invention. *Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1566-67 (Fed. Cir. 1992). As the Supreme Court held in *Markman v. Westview Instruments, Inc.*, this requires a review of “the whole document” (*i.e.*, the patent), in view of “the standard construction rule that a term can be defined only in a way that comports with the instrument as a whole.” 517 U.S. 370, 389 (1996). “Properly viewed, the ‘ordinary meaning’ of a claim term is its meaning to the ordinary artisan after reading the entire patent.” *Phillips*, 415 F.3d at 1321. For this reason, “the specification ‘is always highly relevant to the claim construction analysis,’” and “[u]sually, it is dispositive.” *Phillips*, 415 F.3d at 1315 (citing *Vitronics*, 90 F.3d at 1582).

Courts also consider the prosecution history, which consists of the proceedings before the Patent Office and includes the prior art cited during the examination of the patent. *Phillips*, 415 F.3d at 1317. “[S]tatements made during the prosecution of a patent may affect the scope of the

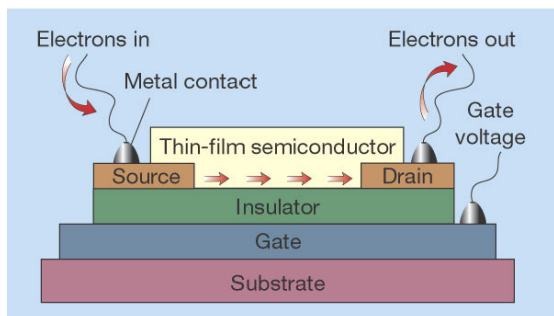
invention.” *Rexnord Corp. v. Laitram Corp.*, 274 F.3d 1336, 1343 (Fed. Cir. 2001). Generally, the prosecution history is relevant if a particular interpretation of the claim was considered and specifically disclaimed during the prosecution of the patent. *Warner-Jenkinson Co., Inc. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 30 (1997).

The court may also consider extrinsic evidence, such as dictionaries, treatises and expert testimony for background information and to “shed useful light on the relevant art.” *Phillips*, 415 F.3d at 1317 (internal citations omitted). But, this type of evidence can often be “less significant” or less reliable than intrinsic evidence in determining “the legally operative meaning of claim language.” *Id.* at 1317.

B. CONSTRUCTIONS FOR DISPUTED TERMS IN LGD’S PATENTS

1. U.S. Patent No. 4,624,737 (JCC Ex. A)

The ‘737 patent describes a specific technique for producing TFTs intended to require fewer manufacturing steps. A TFT is a circuit device having three electrical connections, or



terminals, referred to as the “gate,” “source” and “drain,” as illustrated in the included general diagram. Metal electrodes at the “source” and “drain” are separated by a thin film of semiconductor material, such as silicon. The “gate” controls the flow of current in the “channel”

between the source and drain electrodes, and is separated from the channel by a gate insulator. The current is turned on and off by applying voltage from an external source to the “gate.” The voltage applied to the gate affects the conductive properties of the semiconductor, and hence the flow of current through the TFT channel. *See* Ex. A-3 [U.S. Patent 4,332,075 (Ota et al.)] at 1:8-13; Hatalis Decl., ¶¶ 15-20.

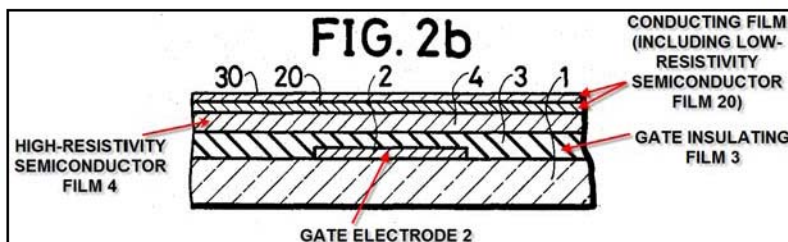
The ‘737 patent purports to improve the technique for building TFTs, and in particular seeks to avoid formation of oxides or other impurities at the interfaces between layers, and to

reduce the number of required “mask” steps. 1:32-53.

a. Gate insulating film (Claim 1) (JCC Ex. A, p. 6)

While similar, there are several significant differences between the competing constructions for “gate insulating film.” First, while LGD’s recognizes the need to provide examples of the gate insulating materials in its construction, it omits the very examples expressly provided in the ‘737 patent. LGD’s construction lists “SiNx” as an example, but the ‘737 patent itself states that “*Beside SiNx, a film of SiOx of a multi-layer film* made of such materials can be used *as said gate insulating film 3.*” 2:36-38 (emphasis added).

Second, CMO’s construction clarifies the location of the gate insulating film relative to the other features of the transistor device: it “span[s] the region from the gate electrode to the high resistivity semiconductor layer.” This location is mandated by the language of claim 1, which states that the gate insulating film, high-resistivity semiconductor film and conducting film are “continuously deposited” (*i.e.*, formed “without intervening films,” as all parties agree) “on said gate electrode and substrate.” In other words, the gate insulating film is between the gate electrode below and the high-resistivity semiconductor film above, as illustrated above in Fig. 2b (annotations added).



In addition, all of the insulating material from the gate electrode to the high-resistivity semiconductor film determines the gate capacitance, and hence the specific electrical characteristics of the gate. Hatalis Decl., ¶¶ 20-24, 41-49; Ex. A-4, at 450-51, 473, 704. Thus, one skilled in the art would understand the gate insulating layer to encompass the region from the gate electrode to the high-resistivity semiconductor film. *Id.*

b. High-resistivity semiconductor film/Low-resistivity semiconductor film/Conducting film (Claim 1) (JCC Ex. A, pp. 7, 9)

The ‘737 patent describes a structure built by the continuous, uninterrupted deposition of several successive films: the “gate insulating film” (discussed above), a “high-resistivity

semiconductor film,” and a “conducting film” (containing a “low-resistivity semiconductor film”). The latter films are shown in Fig. 2b above as film 4 and the combination of films 20 and 30.⁴

The “high-resistivity semiconductor film” includes the “channel” of the TFT, and this clarification is necessary to explain the relationship and location of the channel to the other parts of the TFT. Hatalis Decl. ¶¶ 50-54. The “channel” is mentioned already as part of all parties’ constructions for “source electrode” and “drain electrode” (e.g., “current flows *through the channel* ...”), but the fact that the “high-resistivity semiconductor film” acts as the channel is not otherwise mentioned. The trier of fact must understand the location of the channel, as major goals of the ‘737 patent involve “obtain[ing] a thin-film transistor with small *channel* series resistance” (4:9-12) and “[keeping] the *channel* areas of the thin-film transistor ... safe from damage by cleaning.” 3:2-4.

As to the latter point, the fact that “the channel areas ... are covered with [the] conducting film” in order to keep them “safe from damage by cleaning” (3:2-4) confirms that the “conducting film” of claim 1 “lies adjacent to the channel layer” as provided by CMO’s proposed construction. In addition, the conducting film is sequentially deposited immediately after the high-resistivity film that forms the channel of the TFT, again confirming that the conducting film lies “adjacent to the channel layer.”

c. Depositing on said gate electrode and substrate (Claim 1) (JCC Ex. A, p. 4)

Claim 1 of the ‘737 patent is clear that the successive films are deposited directly: “*on* said gate electrode and substrate,” as shown in Fig. 2b for example (above). While CMO’s construction specifies that the deposited films must be “above and *in contact* with the gate electrode and substrate,” LGD’s construction merely requires that the films be “above and *supported by*” the gate electrode and substrate, without any of the films necessarily *contacting*

⁴ “Conducting film” is used in the ‘737 patent specification to refer to film 30, but in claim 1 it also encompasses the “low-resistivity semiconductor film” 20.

the gate electrode or substrate.⁵

LGD's proposed construction is too broad. Under LGD's construction, all films deposited *anywhere* "above" the gate electrode and substrate (even above several intervening films) could be considered to be "on" the gate electrode and substrate merely because the lower layers "support" the upper ones. Also, LGD ignores the '737 patent's teaching that the "gate insulating film" (which is the layer deposited "on" the gate electrode and substrate) is deposited *immediately* after the gate electrode is formed on the substrate in the "first step" of claim 1 in the "second step." See also 2:10-23, Fig. 2b. CMO's proposed construction of "above and in contact with" thus most accurately captures the relationship between the deposited films and the gate electrode and substrate, and should be adopted.

d. Without exposure to an oxidizing atmosphere/Oxidizing atmosphere (Claim 1) (JCC Ex. A, pp. 10, 11)

The '737 patent teaches that several specific films must be deposited successively "without exposure to an oxidizing atmosphere." This means that they are deposited without exposing them to "an uncontrolled ambient atmosphere which contains oxidizing agents," as provided by CMO's proposed construction.

The '737 patent explains that the prior art might permit oxides or impurities to collect on the silicon interface "as it is exposed to *the atmosphere*." 1:32-40 (emphasis added). According to the patent, the problem with the prior art was that it permitted contact between the silicon and the *uncontrolled ambient atmosphere* which could contain oxides or other impurities, when a sample was moved between fabrication stations. Hatalis Decl., ¶¶ 26, 55-59. To avoid formation of oxides or other impurities, the '737 patent teaches that the various films should be "successively formed ... without exposing them to an oxidizing atmosphere" (2:17-23), *i.e.*, without exposure to oxygen and other impurities in "*the atmosphere*." 1:32-40; 2:33-36 (emphasis added). The '737 patent uses the terms "oxidizing atmosphere" and "the atmosphere" interchangeably, and this meaning is captured in CMO's proposed construction. Hatalis Decl.,

⁵ AUO's construction appears to be silent on this specific point.

¶¶ 55-61.

LGD's proposed construction, by contrast, is overly narrow and vague. For example, it does not focus on isolating the manufacturing process from the outside atmosphere, but instead centers on the amount of oxidation that actually occurs on a film, and whether that would be "detectable." LGD does not, of course, specify the detection method, leaving the scope of the claim to vary depending upon the detection technique as well as the detection threshold, rather than focusing on the point of the patent – isolating the manufacturing process from a potentially contaminating ambient atmosphere. Hatalis Decl, ¶ 62; see also Ex. A-5 [U.S. Patent 4,343,081 (Morin et al)] at 2:33-40 & Abstract (using "outside atmosphere" for same purpose).

e. A source electrode and a drain electrode/Source electrode/Drain electrode (Claim 1) (JCC Ex. A, pp. 15-16)

All three parties have very similar constructions for the above terms, the main difference being that CMO combines them into a single construction, whereas LGD and AUO have separate and partially redundant constructions for them. LGD and AUO's constructions repeat the phrase, "[c]urrent flows through the channel between the source electrode and drain electrode under control of the gate electrode." As such, the jury may be confused as to whether there is more than one source, drain, gate and channel. CMO's combined construction only states this phrase once, thus eliminating the ambiguity.

In addition, the source electrode and drain electrode are introduced as a unit, being formed together in the same step: "a fourth step for selectively forming a source electrode and a drain electrode." *See* Fig. 2d (electrodes 7, 8). Accordingly, they are appropriately defined together.

f. Mask/Source and drain electrodes serving as at least a part of the mask (Claim 1) (JCC Ex. A, pp. 19-21)

While the competing constructions for "mask" have some similarities, they also have significant differences. A mask is the top surface pattern that defines by its edges the boundaries of underlying material to be removed. Elementary semiconductor textbooks explain and

illustrate exactly what a mask is. For instance, one such textbook explains that a mask includes “window patterns” that are “transferred to the wafer surface from a mask” which is used to control deposition and/or etching, and provides a number of tangible examples of how masks are used. Ex. A-6 [*Introduction to Microelectronic Fabrication*, 2nd ed.] at 5, 7-10, 12, 17-19, 23-24. The textbook explains:

Masks contain the patterns of windows that are transferred *to the surface* of the silicon wafer using a process called photolithography...The patterns are first transferred from the mask to a light-sensitive material called photoresist. Chemical or plasma etching is then used to transfer the pattern from the photoresist *to the barrier material on the surface* of the wafer. (*Id.*, at 17, emphasis added).

Thus, the mask involves a barrier material “on the *surface*” of the wafer.

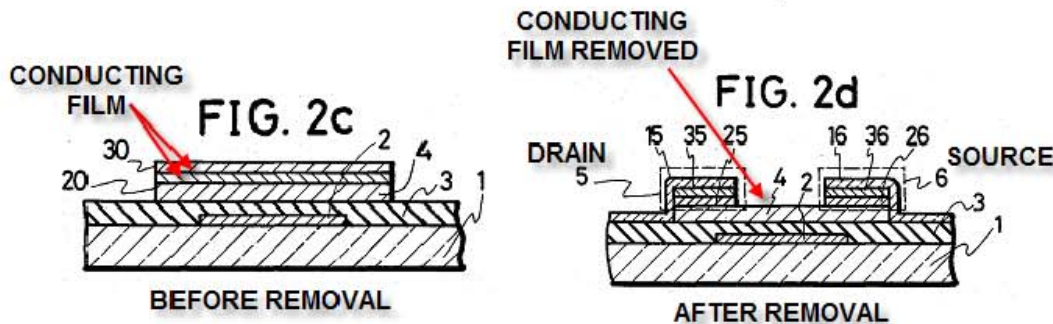
CMO’s proposed construction is consistent with the generally understood meaning of the term “mask,” and specifies that the mask is a “top surface pattern” above one or more layers of material that will be selectively removed “according to the shape of the mask,” that is, the pattern to be transferred to the surface layer. CMO’s construction further specifies that the mask is “made of material that is resistive to the removal technique and defines by its edges the boundaries of the material selected for removal.”

While LGD’s construction refers to a “pattern above a surface” (but not necessarily a “top surface pattern”), there is no requirement in LGD’s construction for the mask to have any influence whatsoever on the shape or boundaries of the material to be removed. LGD’s construction thus ignores the very purpose of the mask, which is to control what material is removed – and what material remains – on the surface layer. CMO’s construction, on the other hand, echoes the teachings of the ‘737 patent, which, as graphically illustrated in Fig. 2d, show how the source and drain electrodes, when serving as part of the mask, define the actual boundaries of the conducting film to be removed.

- g. [A fifth step for] selectively removing said conducting film exposed on said island [with said source and drain electrodes serving as at least a part of the mask] (Claim 1) (JCC Ex. A, p. 17)**

Several disputed claim terms all revolve around the “fifth step” of ‘737 claim 1. The fifth

step involves the “removal” of the conducting film exposed between the source and drain electrodes, as illustrated in the “before” and “after” views in Figures 2c and 2d:



Thus, properly construed, the fifth step means “eliminating all the conducting film in the space between the edges of the source and drain electrodes,” as illustrated in these figures.

The “selective removal” step of claim 1 is carried out with the use of the source and drain electrodes as “part of the mask.” The source and drain electrodes (5, 6) are “spaced apart” in the fourth step of claim 1, thus exposing the conducting film between them, as shown in Figs. 2c-2d above. By removing the conducting film, the source and drain electrodes become electrically isolated. 2:60-66. As illustrated in Fig. 2d, the conducting film between the source and drain electrodes must be eliminated entirely, or the source and drain electrodes may not be electrically isolated which could result in a short between them. Hatalis Decl., ¶¶ 63-68. In fact the ‘737 patent teaches that one should “overetch” beyond the conducting film and into the underlying silicon film 4 (3:7-10), thus ensuring that all of the conducting film is gone, to avoid the possibility of a short.

To emphasize that all conducting material must be removed between the source and drain electrodes, the ‘737 patentee specifically chose the language “selectively *removing*” the conducting film. “Remove” means eliminate (Ex. A-7 [*Webster’s Ninth New Collegiate Dictionary*], at 997), which is precisely what the ‘737 teaches, as illustrated in Fig. 2d above.⁶ See also Ex. A-9 [*Thin Film Processes*] at 407; Ex. A-10 [U.S. Patent 4,404,731 (Poleshuk)] at

⁶ The term “selectively removing” is used in the seventh step as well, where it is likewise necessary to remove (i.e., eliminate) the entire thickness of surface passivation film over the portions of the underlying source, drain and gate electrodes in order to “expose” them.

Fig. 2C, 2:48-62.

CMO's proposed construction accurately captures the teaching of the '737 patent that the source and drain electrodes define (at least in part) the boundaries between which the conducting film is removed, and are thus "part of the mask." By contrast, LGD tries to eliminate the requirement that the source and drain electrodes serve as *part of the mask*. LGD proposes the following construction for the fifth step:

"removing selected regions only of the conducting film on the island region not covered by the *source electrode, drain electrode or mask* wherein the source electrode and drain electrode serve as at least a part of the pattern above *a surface* from which material is to be selectively removed"

LGD's proposed construction improperly tries to differentiate the source and drain electrodes from the "mask" (by allowing removal of selected regions "not covered by the source electrode, drain electrode *or* mask") and allows the possibility that the mask itself defines all of the boundaries of the material to be removed, with no shaping role whatsoever by the source or drain electrodes. This is contrary to the claim language, which requires that the source and drain "*serv[er] as at least a part of the mask.*" As noted previously, a mask defines the boundaries of material to be removed; if the source and drain electrodes do not define those boundaries, then they cannot be deemed "part of the mask."

LGD compounds this error by proposing that the source and drain are merely "part of the pattern" above an undefined "surface," rather than components that actually influence the shape of the conducting film being removed. In fact, under LGD's proposed construction, the source and drain electrodes need not be exposed to the removal process at all, directly contrary to the claim's requirement that the source and drain serve as "part of the mask" for selectively removing conducting film. LGD's vague, overbroad construction should therefore be rejected.

2. U.S. Patent No. 5,019,002 (JCC Ex. B)

The '002 patent discloses a method of manufacturing LCD panels intended to increase the manufacturing yield, decrease manufacturing costs and substantially eliminate fatal display

defects caused by electrostatic discharge (ESD) during manufacture and thereafter. 2:45-51. An example of ESD is the slight shock one feels immediately before one touches a metal doorknob after walking across a carpet. In the LCD manufacturing process, this shock can make the panel unusable by, e.g., causing a short through an insulating layer at the crossover point between row and column lines of the transistor array, or an open circuit (separation) in a row or column line, which could cause an entire row or column to be defective. 4:46-60; 6:26-36. The claimed invention of the '002 patent includes interconnecting row and column lines with guard rings to provide a discharge path to prevent ESD damage, and forming redundant subpixels to minimize the possibility of a fatal display defect. 7:14-24, 6:25-37.

- a. **Claim Terms Previously Construed by the Court - Interconnecting (Claim 1) (JCC Ex. B, p. 3); Outer electrostatic discharge guard ring (Claim 1) (JCC Ex. B, p. 7); Resistance (Claim 1) (JCC Ex. B, p. 8); Removing said outer guard ring and row and column interconnections (Claim 1) (JCC Ex. B, p. 10); Removing (Claim 1) (JCC Ex. B, p. 11)**

The Court has previously construed five of the claim terms at issue. Ex. B-2 [*LG.Philips LCD Co. Ltd. v. Tatung Co.*, C.A. No. 05-292-JJF, June 13, 2006 Memorandum Opinion (“Previous ‘002 Claim Construction”)]. CMO agrees with the Court’s previous constructions. LGD disputes two of the Court’s previous constructions – “interconnecting” and “resistance.”

As an initial matter, LGD should not be permitted to reargue the same constructions that it had already argued to the Court in the previous litigation. The Court has already considered LGD’s arguments and construed these terms. *See Smith & Nephew, Inc., v. Arthrex, Inc.*, No. 2007 WL 1114229, at *2 (D. Or. April 12, 2007) (“[T]he goals of uniformity, consistency, and public notice would be completely undermined if the patentee were allowed to change the meaning of the patent words based on the facts of a given case.”); *Abbott Labs. v. Impax Labs.*, 2003 WL 1563426, at *3 (N.D. Ill. March 26, 2003) (similar).

Moreover, the proper construction for “interconnecting” is “electrically connecting with conductors.” As the Court stated previously, the consistent use of a claim term in the specification appropriately limits the scope of the claim. Ex. B-2 [Previous ‘002 Claim

Construction] at 4-6 (citing *Nystrom v. Trex Co. Inc.*, 424 F.3d. 1136, 1145 (Fed. Cir. 2005)). Here, the applicant consistently used the term “interconnecting” in the patent to mean “electrically connecting with conductors.” *See, e.g.*, 5:65-68 (“The bus lines 82 and 86 are *interconnected* (shorted) at or before the pad 84 and are *interconnected* (shorted) at the opposite ends *by a line or short* 88.”); 6:6-9 (similar); 6:42-43 (“Each pair of the column bus lines 82 and 86 are additionally *interconnected* between each of the subpixels 74, 78, etc. *by respective lines or shorts*.”); Fig. 4, conductors 88, 96. LGD argues that “interconnecting” should mean “electrically connecting with conductive material,” but there is no basis to broaden the scope of the term beyond how it was consistently used in the ‘002 patent.

The proper construction for “resistance” is “a circuit component that has a specified resistance to the flow of electric current and is used to minimize the current surge from an electrostatic discharge.” As the Court previously determined, the only guidance as to the meaning of the term in the patent is the single embodiment in which it appears. Ex. B-2 (Previous ‘002 Claim Construction) at 10-13. The term “resistance” is used consistently as a circuit component of specified resistance that is used to minimize the discharge current surge. 8:23-34, Fig. 7 (showing resistor 228). The term “resistance” was properly construed.

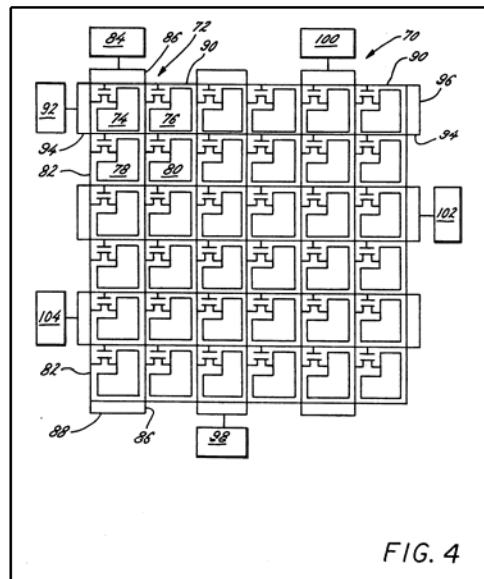
LGD argues that “resistance” should mean “a circuit component designed to provide opposition to electric current flowing through itself and to minimize current surge in the TFT array from electrostatic discharge.” LGD’s modification of the Court’s construction is incorrect, vague, and lacks support in the specification. First, the claims limit the resistance to connecting the interconnected row and column lines to the outer ESD guard ring, so the additional language of “in the TFT array” is incorrect. Second, the proposed construction is unclear as to how a circuit component is “designed to provide opposition to electric current flowing through it.” Third, LGD’s new construction lacks support in the intrinsic record. In the context of the ‘002 patent, a “resistance” is “a circuit component that has a specified resistance to the flow of electric current and is used to minimize the current surge from an electrostatic discharge.”

b. Substrate (Claim 1) (JCC Ex. B, p. 1)

Both CMO and AUO contend that the term “substrate” is unambiguous in the context of the ‘002 patent. The ordinary meaning should apply.

c. Forming a pattern of pixels on said substrate (Claim 1) (JCC Ex. B, p. 1)

CMO contends that the above claim phrase means “forming a repeating configuration of redundant subpixels.” The ‘002 patent states, for example, that Figs. 4 & 6 illustrate “[a] specific subpixel display incorporating an internal guard ring *of the invention*.” 7:47-52. While both Figs. 4 & 6 depict repeating configurations of four subpixels, the patent describes several other similar configurations, e.g., two subpixels, two by four or six subpixels, etc. 5:47-50. The use of multiple, redundant subpixels is needed to address one of



the primary goals for the patent – to prevent the “often fatal display defect ... caused by a defect or open in one of the row or column bus lines which would cause the whole row or column to be out, again resulting in an inoperative display.” 6:25-29. By using multiple, redundant subpixels, an open circuit (or “open”) in a bus line will at most cause one subpixel to be inoperative. An open in a bus line between the ‘002 patent subpixels will result in no visible defects, because the signal is supplied from the opposite end of the bus line through a redundant connection. The redundant subpixels may thus prevent a defect from being a fatal defect. 6:29-37.

LGD argues that this limitation means “depositing and etching a matrix of transparent electrically conductive material to form pixel electrodes above and supported by or in contact with the substrate.” This construction is incorrect because it ignores the context of the patent and the goal of the invention, including the use of subpixels to avoid fatal display defects. *Phillips*, 415 F.3d at 1313 .

d. Forming a plurality of row and column intersecting pixel activation lines (Claim 1) (JCC Ex. B, p. 2)

CMO contends that the above claim phrase means “forming a plurality of row intersecting pixel activation lines and column intersecting pixel activation lines.” This construction provides appropriate grammatical clarification and is fully supported by the claim language and specification. *See, e.g.*, 6:1-18; 6:26-36; 5:58-68; 6:38-50; 7:3-1. AUO’s proposed construction of “forming a plurality of row intersecting pixel activation lines and a plurality of column intersecting pixel activation lines” includes further clarifying language and is an appropriate alternative.

LGD argues that this limitation means “depositing and etching electrically conductive material patterned in rows and columns that control pixels.” This is incorrect because it adds the limitations of “depositing and etching” and “electrically conductive material,” which are unnecessary and do not apply to the context of the ‘002 specification.

e. Interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another (Claim 1) (JCC Ex. B, p. 3)

CMO contends the above claim phrase means “electrically connecting with conductors nearly all, but not all, of said row lines to one another and nearly all, but not all, of said column lines to one another.”⁷ CMO’s proposed construction applies the Court’s prior construction of “interconnecting” (discussed above) and explains, in common language, that “substantially all” means something less than, but close to, all. *See, e.g.*, Ex. B-5 [Merriam-Webster’s Collegiate Dictionary] at 1174 (defining “substantial” as “being largely but not wholly that which is specified”). This is consistent with the language of the claims; had the patentee wanted to encompass all interconnecting lines, it could have used different claim terms (e.g., “all or substantially all”). *Chef America, Inc. v. Lamb-Weston, Inc.*, 358 F.3d 1371, 1374 (Fed. Cir. 2004) (“[W]e construe the claim as written, not as the patentees wish they had written it.”).

⁷ The parties also provide separate constructions, consistent with their constructions for this limitation for the term “substantially all.” CMO combines the discussion of “substantially all” in the construction of the larger claim phrase here.

AUO's proposed construction "substantially all" as "almost all" is similar and is an appropriate alternative construction.

LGD argues that this limitation means "electrically connecting with conductive material all *or* nearly all row lines to at least one other row line and electrically connecting with conductive material all *or* nearly all of the column lines to at least one other column line." This is a clear attempt to rewrite the claim language after the fact to include "all." This is improper.

In addition, LGD took the position in the previous litigation that this claim phrase did not require construction. *See* Ex. B-3 (*LG Philips LCD Co. Ltd. v. Tatung Co.*, C.A. No. 05-292-JJF, Dkt. No. 135, March 8, 2006 Plaintiff's Memorandum In Support Of Its Proposed Claim Constructions at 8). It should not be able to reverse positions now. *Stairmaster Sports/Med. Prod., Inc. v. Groupe Procycle, Inc.*, 25 F. Supp. 2d 270, 280 (D. Del. 1998) (applying judicial estoppel to prevent plaintiff from reversing claim construction position).

f. Inner electrostatic discharge guard ring (Claim 8) (JCC Ex. B, p. 12)

CMO contends that the above claim phrase means "a closed or open ring, or open L or C-shaped conductive line, inside the active matrix display to provide protection from electrostatic discharges." Although this term was not previously construed, this construction flows directly from the Court's construction of "outer electrostatic discharge guard ring" in the previous litigation of the '002 patent (Previous '002 Claim Construction at 7-10), applying it to a ring "inside" the active matrix display, instead of one "outside" the active matrix display. CMO's construction also clarifies that the guard ring is a "conductive" line. As explained by the '002 specification, the ring "provides a discharge path" and accordingly must involve a continuous conductive line.

LGD argues that the inner ESD guard ring is "a closed or open ring, or open L or C-shaped line, inside the source and/or gate pads to provide protection from electrostatic discharge." LGD changes a portion of the Court's construction of outer ESD guard ring from "outside the active matrix display," which it accepts as appropriate for the outer ESD guard ring,

to “inside the *source and/or gate pads*.” This is incorrect because as the specification explains, the gate or source pads could be all on either side of the display (7:18-21) and therefore do not indicate whether a guard ring on the other side of the display was inner or outer. In addition, LGD’s construction introduces ambiguity as to what is inside “the source and/or gate pads.”

g. Shunt switching elements (Claim 8) (JCC Ex. B, p. 13)

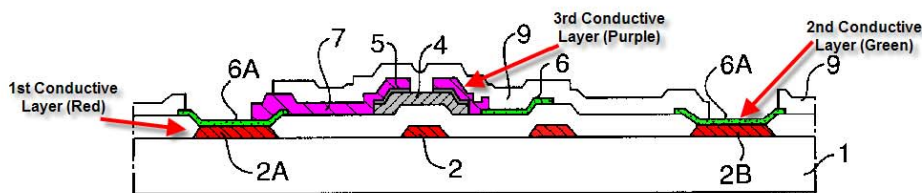
CMO contends that the term “shunt switching elements” means “an active switching element like a shunt transistor or diode.” The ‘002 specification states, for example, that shunt transistors in the disclosed embodiment can be formed as other “active switching elements” and includes the example of diodes. 8:57-59. LGD argues that the term means “shunt transistors, including floating gate, no gate, an oxide below to form a spark gap, or other active switching elements such as diodes,” but introduces many unnecessary new terms that are vague and ambiguous (e.g., “an oxide below to form a spark gap”).

h. Indefinite and Other Claim Terms - Row lines (Claim 1) (JCC Ex. B, p. 5); Column lines (Claim 1) (JCC Ex. B, p. 5); To provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays (Claim 1) (JCC Ex. B, p. 9); Protection from electrostatic discharges (Claim 1) (JCC Ex. B, p. 9); Row and column lines (Claim 8) (JCC Ex. B, p. 6); Row and column activation lines (Claim 8) (JCC Ex. B, p. 10)

The above claim terms are indefinite for lack of antecedent basis. A claim is invalid for indefiniteness if it is “insolubly ambiguous” and not “amenable to construction.” *Novo Indus.s, L.P. v. Micro Molds Corp.*, 350 F.3d 1348, 1358 (Fed. Cir. 2003). The claims require that substantially all row lines are interconnected. The term “said row and column lines” may thus be referring to the substantially all row lines that are interconnected, or the remaining few row lines that are not interconnected. Or the term could be referring to the “row and column intersecting pixel activation lines.” Or the term could be referring to some of the many lines and interconnections shown in the figures. *See, e.g.*, Figs. 5-7. The specification provides no useful guidance as to which of these different possible interpretations is the correct one. Accordingly, the above claim terms are hopelessly ambiguous and cannot be construed.

3. U.S. Patent No. 5,825,449 (JCC Ex. C)

The ‘449 patent relates to a wiring structure for TFTs used in LCD displays. Such devices are constructed using various conductive and insulating materials built up in layers, and patterned into distinct features to form the elements of the transistor or wiring structures. A cross sectional view of a TFT showing multiple layers is illustrated below, described as “Prior Art” in the ‘449 patent:



‘449 FIG. 1f – “PRIOR ART” (Annotations added)

In this figure, the combinations of white and colored features each represent different insulating and conductive layers, respectively. For example, the red features represent a first conductive layer (1:34-37), the green features represent a second conductive layer (1:56-60), and the purple features represent a third conductive layer (1:61-64). The patterning of these layers form parts of a TFT, such as a source pad 2A, gate electrode 2, gate pad 2B, source electrode 7, drain electrode 8 (*see* Fig. 1e), and so on.

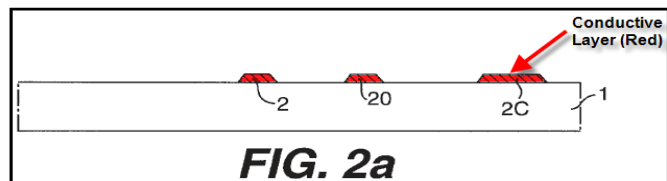
At the time the ‘449 patent was filed, it was common to use the same conductive layers to form both wires and transistor features in an LCD device. The ‘449 patent explains, for example, that “since the source pad for the source wiring is composed of the same material as the gate, its contact resistance ... can be high.” 2:16-18; *see also* 4:1-5; 5:48-51. The ‘449 patent purports to create a TFT and wiring structure using conductive and insulating layers similar to the prior art, but reduces the number of steps to build the structure. 2:19-29, 5:39-47.

a. **Conductive layer (Claims 1, 10, 11) (JCC Ex. C, p. 2)**

The term “conductive layer” is a broad term as used in the ‘449 patent. Properly construed, it denotes “a thickness of electrically conductive material that may include one or more patterned features, all of a single material.” By contrast, LGD argues that this term simply

means “a thickness of electrically conductive material.”

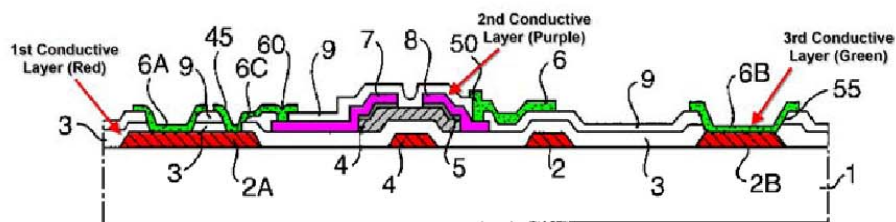
CMO’s construction differs from LGD’s in two key respects. First, it clarifies that the conductive material “may include one or more patterned features.” In other words, the conductive layer includes the various features that are shaped from the layer when or after it is deposited. This is how the ‘449 patent consistently refers to layers. *E.g.*, ‘449 1:34-37; 1:56-60; 1:61-64; 2:37-46; 3:44-47; 4:65 - 5:22; 7:36-39. For example, the ‘449 patent explains in the *Summary of the Invention* that, to accomplish the “objective of the invention,” a device may include “a gate electrode; a gate pad and a source pad formed on the substrate *as a first conductive layer.*” 2:39-40 (emphasis added). The patterned features (gate electrode, gate pad, and source pad in this case) are each part of the “first conductive layer.” A similar example of multiple features formed as a conductive layer is depicted, for example, in ‘449 Fig. 2a (annotation added), inset.



The ‘449 patent makes it clear that these features are part of the same conductive layer:

[A] *conductive layer* is formed on a transparent glass substrate 1 and patterned to form a *gate electrode 2*, a *storage capacitor electrode 2D*, and a *gate pad 2C*, all of the same material. 3:44-47.

A nearly identical description is used to describe the various conductive layers shown below in Fig. 3 (annotated with labels below):



‘449 FIG. 3

See 4:65 – 5:1; 5:6-8; 5:16-22. Claim 10 also confirms that a conductive layer may include one or more patterned features, as it recites “*a first conductive layer ... including: a gate electrode, a gate pad, and a source pad*[.]” 7:36-39 (emphasis added). Thus it is clear from the specification of the ‘449 patent that the term “conductive layer” may encompass “one

or more patterned features.” See also Hatalis Decl., ¶¶ 77-79.

The ‘449 patent also explains that the various patterned features in a conductive layer are “*of the same material*.” 3:44-47 (emphasis added). CMO’s proposed construction thus likewise clarifies that the patterned features of the conductive layer are made of the same material. Features within a layer must be made of the same material, moreover, because these features all originate from the same “thickness” of electrically conductive material, and are “simultaneously patterned” or “formed at the same time.” 1:61-64, 4:50-53; Hatalis Decl., ¶¶ 80-81.

On the other hand, LGD’s proposed definition of a conductive layer as simply a “thickness of electrically conductive material” is incomplete. It fails to account for the fact that a single conductive layer can include multiple patterned features, or that the material would be the same for all the patterned features.

b. [Wherein] one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor (Claim 1) (JCC Ex. C, p. 7)

Perhaps because the above term (the “wherein” clause) first arose in a dispute on the eve of trial in the prior LGD/CPT litigation, the parties to that case apparently overlooked critical aspects of the file history that illuminate the meaning of this term. The parties’ oversight led to a flawed result. The prior construction incorrectly provided that “*one, but not both*, of the first and second conductive layers” is connected to one of a plurality of terminals of a TFT.⁸ Properly construed, however, the phrase encompasses either one *or* both conductive layers being connected to one or more terminals of a TFT.⁹

The clause in question was simultaneously added during prosecution to issued claims 1, 2 and 6 of the ‘449 patent, in order to gain allowance. These three claims appeared originally as application claims 7, 8 and 11, respectively. Ex. C-3, at 1-4 [Amendment]. All of these claims

⁸ In the ‘449 file history, the Applicant explained that the “terminals” of a TFT “correspond to the gate, source and drain” of a TFT. Ex. C-3 [Amendment], at 5.

⁹ CMO’s full proposed construction for this term is: “The first conductive layer is connected to the gate, source or drain of a thin film transistor, and/or the second conductive layer is connected to the gate, source or drain of the thin film transistor.”

involve at least two conductive layers connected by a third conductor through contact holes. In adding the subject limitation (the “wherein” clause) to each of the three claims, the Applicant clearly explained what was meant by the addition of the language. Because the amended language was first added to claim 6 (11), the Applicant’s primary explanation for this change came in connection with the amendment of claim 6 (11):

“By this Amendment, Applicant has amended claim 11 *essentially to include the recitations of canceled claim 12.*” Ex. C-3, at 5 (emphasis added).

Canceled claim 12, in turn, indisputably demonstrates that *both* the first and second conductive layers can be connected to terminals (i.e., gate, source or drain) of a TFT:

12. A liquid crystal display device in accordance with claim 11, wherein said *first conductive layer is a gate electrode* and said *second conductive layer is a source electrode.* Ex. C-4, at 15-16 (emphasis added).

In the case of claim 12, both the first and second conductive layers are connected to a terminal (gate and source respectively) of a TFT. Because the “wherein” clause “essentially includes” the recitations of original application claim 12, it too must be broad enough to include the situation where *both* conductive layers are connected to terminals of a TFT.

When making the same amendment to claim 1 (7) at issue here, the Applicant referred back to the same amendment already made to claim 6 (11):

“Even if the Examiner’s assertion is correct, Kakuda et al. fails to render obvious claims 7, 9 and 13. In particular, *claim 7, as amended, recites that a wiring structure similar to claim 11 includes one of the first and second conductive layers being connected to one of a plurality of terminals of a thin film transistor*, which Kakuda et al. fails to disclose or suggest *as discussed above with respect to claim 11.*” Ex. C-3, at 7 (emphasis added).

Thus, the same explanation as Applicant provided for claim 6 (11) was also intended to apply to claim 1 (7).

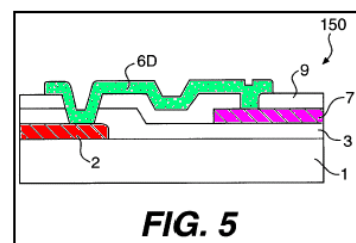
Because claim 12 was canceled and “essentially included” in the “wherein” clause added to claims 1 (7) and 6 (11), it would be manifestly unreasonable to interpret the “wherein” clause

as **excluding** the subject matter of claim 12.¹⁰ Such a construction would be too narrow and undermine the important public notice function of the file history. *Springs Window Fashions LP v. Novo Indus., L.P.*, 323 F.3d 989, 995 (Fed. Cir. 2003) (“The prosecution history constitutes a public record of the patentee’s representations concerning the scope and the meaning of the claims, and competitors are entitled to rely on those representations when ascertaining the degree of lawful conduct”).

CMO’s proposed construction is also consistent with the claim language as well as the intent of the ‘449 patent. Claim 1 starts with the broad open-ended term “comprising” meaning that additional elements can be included within the claim scope. *AFG Indus., Inc. v. Cardinal IG Co., Inc.*, 239 F.3d 1239, 1244-45 (Fed. Cir. 2001). Thus, although the “wherein” clause calls for a minimum of “one” of the two conductive layers to be connected to one of the terminals of a TFT, the use of “comprising” in the claim would not limit the scope of the claim to such a configuration, and permit connecting the other conductive layer to a terminal of a TFT as well.

CMO’s construction is also consistent with the goal of the ‘449 patent to utilize the same conductive layers for fashioning both wiring and TFT structures (e.g., 2:16-29), while LGD’s construction would preclude both the first and second conductive layers from being used to form or connect to relevant TFT features. Such a cramped reading overlooks a key purpose of the ‘449 patent to use a limited number of conductive layers to serve both as wiring and to form or connect to TFT structures. *See, e.g.*, 2:16-18; 4:1-5; 5:48-51

In addition, Figs. 4 and 5 show an embodiment of “the present invention” in which the first and second conductive layers are **both** connected to different terminals of a TFT. Specifically, the



¹⁰ The Federal Circuit has touted the importance of statements made in the prosecution history to ascertain at the intent and meaning of claim terminology. *See Phillips v.* , 415 F.3d at 1317 (“[T]he prosecution history can often inform the meaning of the claim language by demonstrating how the inventor understood the invention ...”); *Lemelson v. General Mills, Inc.*, 968 F.2d 1202, 1206 (Fed. Cir. 1992) (“The prosecution history gives insight into what the applicant originally claimed as the invention ...”).

first conductive layer (2) is connected to one terminal of a TFT (gate), while the second conductive layer (7) is connected to another terminal (source).¹¹

LGD's construction would exclude this preferred embodiment of the '449 patent, but such a construction is "rarely, if ever, correct." *Vitronics Corp. v. Conceptronics, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996); *MBO Labs., Inc. v. Becton, Dickinson & Co.*, 474 F.3d 1323, 1333 (Fed. Cir. 2007). This is not one of those rare cases. The evidence is overwhelming that either one or both the first and second conductive layers may be connected to one (or more) of the terminals of a TFT.

c. Gate pad/Source pad (Claims 10, 11) (JCC Ex. C, pp. 12, 13)

The proposed constructions are very similar for the terms "gate pad" and "source pad," except that, as compared to LGD's proposed construction at least, CMO's constructions include the highlighted language at the tail end of each clause below:

Gate Pad	Source Pad
A portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive a gate signal <i>from a gate driving circuit</i>	a portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive a data signal <i>from a data driving circuit</i>

AUO's construction, while slightly different, also includes the same language at the end. In both cases, the added language is necessary to clarify that the gate signal and data signal are received from particular circuitry intended to interface with the gate pad and source pad, respectively.

These constructions are based directly on the '449 specification, which explains:

"Gate Pads 630 and Data [Source] Pads 640 are connected to the gate lines and data lines to receive datas [sic] from *gate driver* and *data driver* respectively." 1:27-30 (emphasis added).

Claims 10 and 11 relate not just to a TFT but to an entire "liquid crystal display device"

¹¹ Figs. 4 and 5 illustrate an application of the earlier Fig. 3 TFT embodiment, and show that as a matter of principle the '449 patent intended to embrace configurations with the first and second conductive layers each connected to a terminal of a TFT.

or method for making the same, and the gate driving circuit and data driving circuit play a significant role in controlling operation of the LCD device.

In fact, so clear is this point that LGD itself *proposed the same language* in the prior case involving the ‘449 patent, and that language was adopted by Judge Consuelo Marshall’s claim construction ruling. Ex. C-5 at 17; Ex. C-6 at 162-168. Having advocated for this language once before, and prevailed, LGD should not be allowed to do an about-face and argue the exact opposite here. Indeed, notions of issue preclusion as well as judicial estoppel would prevent LGD from changing its position before this Court. *Smith & Nephew, Inc., v. Arthrex, Inc.*, No. CV04-29-MO, 2007 WL 1114229, at *2 (D. Or. April 12, 2007) (“[T]he goals of uniformity, consistency, and public notice would be completely undermined if the patentee were allowed to change the meaning of the patent words based on the facts of a given case.”); *Abbott Labs. v. Impax Labs.*, 2003 WL 1563426, at *3 (N.D. Ill. March 26, 2003) (similar); *Stairmaster Sports/Med. Prod.*, 25 F. Supp. 2d at 280 (applying judicial estoppel to prevent plaintiff from reversing on claim construction position); Ex. C-8.

d. A source electrode and a drain electrode/Source electrode/Drain electrode (Claims 10, 11) (JCC, Ex. C, pp. 18, 19)

The claim construction issues for these terms are the same for the ‘449 patent as in the ‘737 patent. Like the ‘737 patent, the ‘449 patent introduces these terms as a unit (“*a source electrode and a drain electrode* on said semiconductor layer” in claim 10 and “*patterning said second conductive layer to form source electrode and a drain electrode* on said active layer” in claim 11), and they are therefore appropriately treated as such. In addition, CMO’s construction is simpler and less repetitious than LGD’s and AUO’s separate constructions for these terms, and eliminates potential ambiguity in those dual constructions as described in relation to the ‘737 patent.

e. Active layer (Claims 10, 11) (JCC Ex. C, p. 23)

While the constructions of CMO and LGD are similar for “active layer,” largely based on the prior construction from the LGD/CPT litigation, LGD surreptitiously drops the article “the”

before “semiconductor layer” – thus not only deviating from the prior construction, but also injecting significant ambiguity into whether the claim refers to the previously recited “semiconductor layer” in the claim, or some other unspecified semiconductor layer. LGD’s attempt to inject such ambiguity should be rejected. In addition, CMO’s definition specifies that the active layer is “of a thin film transistor” – hardly a point that can be disputed by LGD. Accordingly, CMO’s definition is the most accurate and precise, and should be adopted.

4. U.S. Patent No. 6,803,984 (JCC Ex. E)

The ‘984 patent discloses using a single production line in combination with a liquid crystal manufacturing technology known as “dropping.” 1:12-16; 3:63-4:13. The *Background* section of the ‘984 patent describes that, in the prior art fabrication process for LCD devices using the liquid crystal dropping method, the two substrates making up the LCD panel (the TFT and CF substrates) are prepared in different processing lines. 2:39-53. The CF substrate is loaded into a “seal dispenser,” whereupon sealant is applied to the periphery of the substrate. 2:54-59. On a different processing line, the TFT substrate is loaded into a liquid crystal dispenser (“LC dispenser”), in which a series of drops of liquid crystal material are deposited on the substrate. 2:3-3:12. The substrates are then attached together downstream sealing the liquid crystal material inside. 3:12-21.

The purported invention of the ‘984 patent was to process pairs of alternating TFT and CF substrates together on a single production line, by, among other things, moving both substrates through the seal dispenser (but only depositing sealant on one of the substrates), and then passing both substrates through the LC dispenser (but only depositing liquid crystal material on one of the substrates). 5:39-49, 55-61. According to the ‘984 patent, the single production line increases “spatial efficiency,” lowers costs by not needing “two sets of expensive equipment,” and avoids “efficiency losses due to different processing times between the two production lines (*i.e.*, line unbalance).” 3:37-53.

a. On a single production process line (Claims 1-3) (JCC Ex. E, p. 2)

The term “on a single production process line” means: “on a line structure for processing the substrates in only one direction without branching.” The ‘984 specification describes the production line as “a single line structure for progressing the [alternating CF and TFT substrates through] liquid crystal cell process.” 5:23-27. The ‘984 specification describes (and the purported benefits of the ‘984 patent involve) using a single production line of equipment through which all panel components move, as opposed to a production line with “parallel” processing through the use of branches (*i.e.*, where components do not all follow the same production line), parallel assembly lines with the same sets of steps, or side assembly lines in which some components are diverted off the “single line” structure. *See* Exs. E-3, E-4. LGD’s proposed construction,¹² however, is so vague and general as to encompass all of these potential arrangements of assembly lines, none of which use a “single line structure” as required by the ‘984 patent.

Indeed, the ‘984 patent expressly discourages the use of parallel, branch, or side assembly lines. The *Background* section discusses the problems of “parallel” processing, including loss of equipment and spatial efficiency, and efficiency losses resulting from differences in processing times for the separate CF and TFT lines. 3:37-43. The *Summary of the Invention* discusses how these problems are avoided by sending both the TFT and CF substrates through the same seal coating and liquid crystal dispensing machines. 3:61-4:13. The ‘984 patent reinforces that both substrates pass through the “sealing material coating step” (6:32-35) and “[liquid crystal] dropping step” (6:39-41), which take place in a “seal dispenser” (2:54-56) and a “LC dispenser” (2:63-66), respectively. Thus, CMO’s construction most closely matches the purpose and operation of the alleged invention.

b. A sealing material coating portion/A liquid crystal dispensing portion (Claims 1-3, 5) (JCC Ex. E, pp. 4, 6)

“A sealing material coating portion” and “a liquid crystal dispensing portion” mean: “a

¹² LGD’s construction is “on a production line where the processing equipment is arranged along a common path for performing the liquid crystal cell processes.” JCC Ex. E, p. 3.

machine for coating sealing material” and “a machine for dispensing liquid crystal material” respectively. As discussed above, the ‘984 patent describes both substrates passing through the “sealing material coating step” (6:32-35) and “[liquid crystal] dropping step” (6:39-41), which take place in a “seal dispenser” (2:54-56) and a “LC dispenser” (2:63-66), respectively.

During prosecution, the patentee differentiated “Admitted Prior Art” on the basis that such art disclosed that “if a substrate passes through a process portion, the corresponding process is always performed.” Ex. E-2 (1/6/04 Resp. at 4). In the alleged invention, substrates pass through “process portions” without the corresponding process being performed. *Id.* The claimed “process portions” (“sealing material coating portion” and “a liquid crystal dispensing portion”) are the equipment for performing the corresponding steps (“seal dispenser” and a “LC dispenser”). Any construction, such as the one LGD proposes,¹³ that allows the substrates to pass through a “process portion” without passing through the actual “seal dispenser” and a “LC dispenser” contradicts binding positions of the patentee taken to gain allowance of the claims.

c. Passing...through...in serial order (Claim 1) (JCC Ex. E, p. 3, 5)

“Passing ... through ... in serial order” means: “providing ... one after the other without anything in between, in at one end, and out at the other end ... in which the same order of the first and second substrates is maintained throughout the ... process.” The common meaning of “passing through” is passing something in one side and out the other. *See* Ex. E-5. The common meaning of “serial order” is one after the other, without gaps. *See* Ex. E-6. Moreover, the ‘984 patent describes that the alternating sequence of the TFT and CF substrates, *i.e.* the serial order, is maintained throughout the processing. 3:61-4:13; Fig. 2-4.

CMO’s proposed construction incorporates these aspect of the invention. LGD’s proposed construction,¹⁴ in contradiction to the ‘984 specification, would allow LGD to argue that the substrates do not need to pass “through” the actual seal coating and liquid crystal

¹³ LGD’s construction is “a portion of the single production process line where the sealing material is selectively applied.” JCC Ex. E, p. 5.

¹⁴ LGD’s construction is “passing ... along” JCC Ex. E, pp. 4, 6.

dispensers and that the order of the substrates does not need to be maintained during the processing in order to fall under the scope of the claims.

d. A second substrate (Claim 1, 5, 10) (JCC Ex. E, p. 1)

“A second substrate” means: “the substrate immediately following the first substrate.” The ‘984 patent describes that the TFT and CF substrates are provided in an alternating sequence: “The TFT substrate and the color filter substrate are alternately provided into a production line....” 5:23-25. The ‘984 patent also describes processing the TFT and CF substrates as a “pair.” 7:26-34. Again, CMO’s proposed construction makes this aspect of the claims clear. No construction of “first substrate” is required.

5. U.S. Patent Nos. 5,905,274 (JCC Ex. F); 6,815,321 (JCC Ex. G); 7,176,489 (JCC Ex. H)

The ‘274, ‘321 and ‘489 patents are related and will be referred to collectively as the ‘274 patent.¹⁵ The ‘274 patent discloses a thin film transistor (“TFT”) with a gate electrode that has two metal layers. 3:21-26. As explained earlier (in Section B(1)), the “gate” controls the flow of electrical current through a TFT. It is desirable to construct a transistor gate from aluminum to reduce wiring resistance. 1:17-19. Gates constructed from aluminum may cause defects known as hillocks. *Id.* To overcome the problem of hillock a layer of molybdenum may be formed on the aluminum to create a double layered gate. 1:20-22. The creation of a double layered gate can result in a severe step that deteriorates the step coverage of a later formed gate oxide layer. 1:27-34. The background section of the patent describes “a related” fabrication process that created a double step in a double-layered gate. 1:43-2:65. Based on an assumption, the named inventors believed that the first metal layer was wider than the second metal layer by a value larger than or equal to 4 μm . 2:14-21. The related fabrication process included using a different photoresist to form each layer of metal. 1:48-65.

The purported invention of the ‘274 patent is to fabricate a double-layered metal gate where the difference in widths between the first and second metal layers is greater than 1 μm but

¹⁵ All references to the specification and drawings will be to the ‘274 patent.

less than 4 μm . 4:45-51. The '274 patent discloses a fabrication process in which the second metal layer is deposited directly on the first metal layer and a photoresist with a specified width is formed on the second metal layer. 3:48-52. The metal layers are then etched using the photoresist as a mask. 3:52-55.

a. Double-layer structure ('274 patent, Claims 1, 4) (JCC Ex. F, p. 3)/Double-layered metal gate ('321 patent, Claim 7; '489 patent, Claim 1) (JCC Ex. G, p. 4; Ex. H, p. 3)

CMO submits that these terms mean: "a gate that has only two metal layers." The word "double" defines the number of layers in the structure, two. The claim does not recite a structure with a triple layer, or a plurality of layers, but specifically recites a double layer, meaning a structure with two layers. This construction is supported by the intrinsic evidence of the patents.

The only gate structure that is disclosed or contemplated by the patents is a double-layer (i.e., two layer) structure. The Summary section discusses embodiments and methods for making this double-layered gate: "[t]he preferred embodiments of the present invention also provide a method of fabricating a thin-film transistor that simplifies the process for forming a double metal layer gate." 3:27-29. The Detailed Description section only describes a double layered gate and various alternate processes for fabricating a gate with two layers: "[t]he gate 49 has a double-layered structure including the first and second metal layers 43 and 45 disposed on the substrate 41." 4:32-34. "The first and second metal layers 43 and 45 resulting from the single photoresist step process described above form a gate 49 having a double-layered metal structure." 6:27-29. The '274 patent family is all about double-layered gates.

Additionally, the patentee distinguished the claimed two layered gate from a three layered gate of the prior art. During prosecution of the '274 patent the PTO rejected the claims in view of two references, one of which was U.S. Pat. No. 5, 036,370 issued to Miyago et. al. ("Miyago"). Miyago disclosed a gate with three layers, an aluminum ("Al") layer, a molybdenum ("Mo") layer and a layer of tantalum ("Ta"). In responding to the office action the patentee made the following statement:

“Miyago does use an aluminum layer in a double-layered gate and does recognize a hillock problem which occurs along a top surface of a bottom aluminum layer located between the aluminum layer and a top layer. Miyago provides an entirely different solution by providing a clad structure for causing the top-surface hillock problem to be reduced. More specifically, Miyago teaches that in order to solve the top-surface hillock problem, a first tantalum layer is put on the Al-Mo double layer structure then a TaOx layer is put on the Ta layer.” Ex. FGH-1.

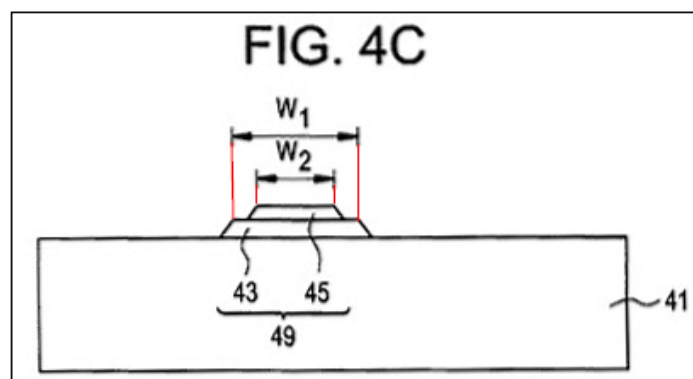
The three-layered Miyago gate was characterized as an Al-Mo double layer with a layer of tantalum on top. By the patentee’s own admission a three layered gate is not within the scope of the claims. Just as a “double” in baseball means two bases, not three, the double-layered metal gate/structure should be construed as a gate with two layers.

- b. **The first metal layer being wider than the second metal layer by about 1 to 4 μm (‘274 patent, Claims 1, 4) (JCC Ex. F, p. 8)/The first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4 μm (‘321 Patent, Claim 16) (JCC Ex. G, p. 13)/A total width of the first metal layer being greater than a total width of the second metal layer by about 1 to 4 μm (‘321 patent, Claim 7; ‘489 patent, Claim 1) (JCC Ex. G, p. 6; Ex. H, p. 5)**

These terms mean “the top surface of the first metal layer has a width that is about 1 to 4 μm wider than a width of the top surface of the second metal layer to form a double step gate. A double step gate is a structure where not all of the top surface of the first metal layer is covered by the second metal layer.” The difference between the parties’ constructions is that CMO provides clarity and LGD leaves and introduces ambiguity.

Because the metal layers may have a taper, the top surface may be shorter than the bottom surface of a layer. *See* Fig. 3. To determine the scope of the claims it is essential to understand where to measure the widths of the layers. There are two pieces of evidence that answer this question.

Reproduced is an annotated copy of Figure 4C from the ‘274 patent. The drawing shows a first metal layer 43 and a second metal layer 45. Also shown are width dimensions W_1 and W_2 that



correspond to the first and second layers, respectively. As shown by the red annotations, when the width dimension lines are extended down to the gate, the lines correspond with the top surfaces of the first and second metal layers. Figure 4C supports a construction that the widths should be measured relative to the top surfaces of the first and second metal layers.

LGD's own statements to the British Patent Office confirm that the width measurements in the '274 patent are made along the top surfaces of each layer. The '274 patent family originated from a single Korean application. In addition to filing in the U.S., LGD had also filed a corresponding application in Great Britain. The British Patent Office issued an office action requesting a clarification on where to measure the claimed widths. Ex. FGH-1 (United Kingdom Application, 9804417.5, Office Action, May 21, 1998 at 2). LGD filed a response with the following statement:

“The understanding that this measurement relates to the widths of the tops of each of the two layers may be further clarified, if necessary, by referring to the diagrams, specifically Figure 4C.” Ex. FGH-1 (United Kingdom Application, 9804417.5, Response, March 4, 1999 at 3).

CMO's proposed construction thus tracks exactly what LGD told the British Patent Office about the location of the measurements.

Creating a second metal layer that is smaller than the first metal layer creates a double step. 4:45-51; 5:25-34; 6:40-45. A double step is where a portion of the top surface of the first metal layer is not covered with the second metal layer. *See* Fig. 4C. LGD's construction appears to cover this concept but leaves some ambiguity. In relevant part LGD's construction is “the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer.” The insulating layer covers not only the exposed top surface of the first metal layer but also the tapered side surfaces of the first layer. *See* Fig. 3, insulating layer 51. LGD's construction is open to multiple interpretation of widths. The width could be only the top surface of the first metal layer, the top surface plus the length of the tapered surfaces, or the width of the

bottom surface of the first layer. CMO's construction is clear, the widths should be measured relative to the top surface of the first metal layer and the top surface of the second metal layer, and the exposed portions of the first metal layer are on the top surface of the first layer.

c. Forming a single photoresist having a predetermined width on the second metal layer ('321 patent, Claim 16) (JCC Ex. H, p. 9)

CMO's proposed construction, "the photoresist is deposited in direct contact with the second metal layer," clarifies that there is no intermediate layer between the photoresist and the second metal layer. This is supported by the intrinsic evidence. *See* 5:55-62; Fig. 4B. This construction is also consistent with other claim terms that include the word "on" or "thereon." For example, a number of claims recite a second metal layer on or thereon the first metal layer ('274 patent, claims 1 and 4; '489, claim 1; '321 patent, claims 7 and 16). All parties agree that these terms mean that the first metal layer is in direct contact with the second metal layer. *See* JCC Exs. F, p. 3; G, p. 2-3; and H, p. 5.

6. U.S. Patent No. 7,218,374 (JCC Exhibit I)

The '374 patent discloses a specific way of sealing together the two substrates that make up an LCD panel during manufacture of an LCD device. According to the background section of the specification, a dispensing device applies sealing material around the edges of the active region of one substrate to confine the liquid crystal. 2:5-13; Figs 1A-1C. The high viscosity of the sealing material causes it to concentrate at the nozzle of the dispensing device prior to its application. 2:40-46. Thus, upon initial application, the nozzle typically applies an excessive amount of sealing material (*i.e.*, a "blob") upon the substrate. *Id.* When the other substrate is attached to this substrate, the blob of excessive sealant spreads into the active region of the substrate, which contaminates the liquid crystal. 2:47-54.

The '374 patent attempts to avoid this problem by simply applying the initial blob of sealant away from the active region of the LCD display. Figure 3C is illustrative. By applying excess sealant 70A (referred to as "auxiliary sealant" or "supplementary sealant") to

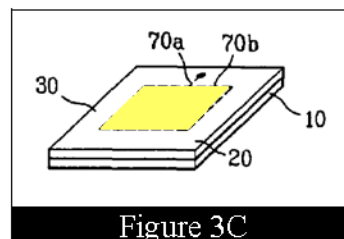


Figure 3C

the non-active region of the substrate before applying the “main sealant” 70B, the blob of excess sealant forms away from the active region (highlighted in yellow). Therefore, when the substrates are attached, the blob of excess sealant does not contaminate the liquid crystal. *See, e.g.*, 3:9-34; 5:7-20.

a. Main sealant/Auxiliary sealant (Claims 1, 21) (JCC Ex. I, pp. 1-3)

CMO’s construction for “main sealant” is “sealant material that is necessary for confining liquid crystal from leaking out between the substrates.” CMO’s construction for “auxiliary sealant” is “sealant material that is not necessary for confining liquid crystal from leaking out between the substrates.” In accord with basic principles of claim construction, CMO’s constructions reflect the specific teaching of the specification:

[T]he supplementary UV sealant does not perform the ordinary the (sic) function of a sealant, that is, it does not prevent the liquid crystal from leaking out. While the main UV sealant acts as a sealant to confine the liquid crystal.¹⁶ 3:20-24.

LGD and AUO’s constructions fail to reflect this teaching. For example, LGD’s and AUO’s constructions for “auxiliary sealant” merely focus on where an “auxiliary sealant” might be located on the substrate – *i.e.*, “in an area outside of the main sealant.”¹⁷ In so doing, LGD and AUO merely mimic word-for-word their proposed constructions for a subsequent claim limitation, “the auxiliary sealant is formed in a dummy region,” which they construe as “the auxiliary sealant is formed in an area outside of the main sealant.”¹⁸ Thus, LGD and AUO’s constructions for “auxiliary sealant” render this subsequent claim limitation merely superfluous, which violates a fundamental tenet of claim construction. *See, e.g., Stumbo v. Eastman Outdoors, Inc.*, 508 F.3d 1358, 1362 (Fed. Cir. 2007) (“construing the word ‘vertical’ as

¹⁶ The specification uses the terms “auxiliary sealant” and “supplementary sealant” interchangeably. *See, e.g.*, 3:9-40.

¹⁷ LGD’s construction for “auxiliary sealant” is “sealant deposited in an area outside of the main sealant.” AUO’s construction is “a segment of sealant that extends from the main sealant and is outside the enclosure of the main sealant.” *See* JCC Ex. I, p. 3.

¹⁸ The parties dispute the precise wording of the construction for “dummy region” but the constructions are substantially the same. *See* JCC Ex. I, p. 4.

[plaintiff proposes] would render [other claim terms] superfluous, a methodology of claim construction that this court has denounced”).

Moreover, LGD’s construction for main sealant – “sealant material that encloses the display region” – is overbroad and encompasses within its scope certain sealant that should be considered “auxiliary sealant” according to the specification of the ‘374 patent. The flaw in LGD’s construction is best exemplified by envisioning a substrate with a sealant pattern having concentric sealants, like 2a and 2b depicted in Fig. 4 of LGD’s prior art reference, U.S. Patent No. 6,573,968 (Ex. I-2) cited in the prosecution history of the ‘374 patent. Although both sealants 2a and 2b enclose the display region (highlighted in yellow), sealant 2b is not in contact with, and does not actually “confine,” the liquid crystal, which is the specification’s stated purpose of main sealant. 3:20-24. However, sealants like sealant 2b are nonetheless encompassed within the scope of LGD’s construction for “main sealant,” in contradiction of this specific teaching of the ‘374 patent.¹⁹

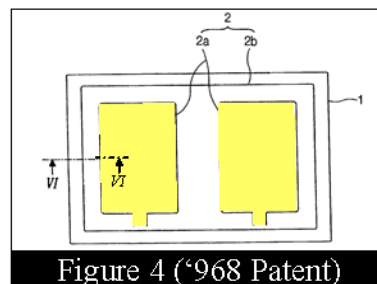


Figure 4 (‘968 Patent)

b. Wherein the auxiliary UV sealant is formed in a dummy region and extends outside from the main UV sealant (Claim 21) (JCC Ex. I, p. 5)

CMO’s construction is “wherein the auxiliary UV sealant is formed in an area outside the boundary of the main UV sealant beginning from the main UV sealant and moving outward.” The parties largely agree regarding the proper construction for the first part of this claim element. JCC Ex. I, p. 5. However, only CMO’s construction accounts for the additional claim language, “and extends outside from the main UV sealant.” AUO, with its construction, altogether ignores this claim language, while LGD construes it as “and is joined to the main sealant,” a limitation that bears no relation to the plain import of the claim terms. *See Phillips*, 415 F.3d at 1312 (“[I]t is unjust to the public, as well as an evasion of the law, to construe [an invention] in a manner different from the plain import of its terms.”).

¹⁹ Consistent with the understanding of one of skill in the art, U.S. Patent No. 6,573,968 also refers to sealant 2b not as a “main sealant” but as an “auxiliary seal line.” Ex. I-2 at 3:3.

c. Wherein the auxiliary sealant and the main sealant are contiguous (Claim 1) (JCC Ex. I, pp. 5-6)

CMO's construction – "wherein the auxiliary sealant touches but does not overlap the main sealant" – reflects the meaning of the claim language, while remaining true to the specification. The term "contiguous," which never appears in the patent specification, is commonly defined as "being in actual contact" or "touching along a boundary or at a point." Ex. I-3 (*Merriam Webster's Collegiate Dictionary*). True to this meaning, every figure and description of "auxiliary [and] main sealant[s]" in the patent specification depicts the sealants touching at a point with no overlap. *See e.g.*, Figs. 3B-6; 3:65-4:10. LGD attempts to construe "contiguous" as "deposited in a continuous manner." However, the term "contiguous" refers to the relative positioning of the sealants on the substrate, not the manner in which they were applied.²⁰

d. Applying a liquid crystal on one of the lower and upper substrates (Claims 1, 21) (JCC Ex. I, p. 7)

Because this claim language is clear on its face, CMO believes it should be given its plain and ordinary meaning. With its proposed construction, LGD has improperly attempted to replace the term "applying," with the more limiting "depositing," despite uniform references in the specification to "applying [liquid crystal]," *see, e.g.*, 1:51-52; 2:6; 2:11; 3:31; 5:30, and not a single reference to "depositing [liquid crystal]."²¹

C. CONSTRUCTIONS FOR DISPUTED TERMS IN CMO'S PATENTS

1. U.S. Patent No. 5,619,352 (JCC Ex. R)

The '352 patent discloses a device called an "optical compensator" that can improve the

²⁰ AUO's proposed construction, "physically connected," disregards the principle of claim differentiation in that it is essentially identical to its constructions for, and renders superfluous, the claim term "connects," which appears in the same claim 1 at 8:43, as well as the claim term "contacts," which appears in dependent claim 20 at 10:8. *See* JCC Ex. I, pp. 4, 7.

²¹ Similarly, LGD attempts to add an unsupportable "depositing" limitation to its construction for the claim elements "forming a main sealant," "auxiliary sealant," "formed in a dummy region," "the auxiliary sealant and the main sealant are contiguous," and "preparing a lower substrate and an upper substrate." JCC Ex. I, pp. 1, 3-6.

contrast ratio and gray scale stability of LCDs. 10:49-53. LCD displays include a liquid crystal layer located between a polarizer and an analyzer. 3:65-4:3. The liquid crystal layer is sandwiched between a pair of substrates with first and second transparent electrodes. 4:17-22. The electrodes are used to apply a voltage across the liquid crystal layer. *Id.* When a voltage is not applied, the liquid crystal layer rotates the light 90° so that light can pass through the analyzer and the display looks white. 4:43-51; Fig. 1A. When a voltage is applied, the orientation of the liquid crystal layer changes causing the analyzer to block light. This makes the display look black. 4:52-57; Fig. 1B. Thus, when a voltage is applied the normally white display is black, and when not applied the display emits light. 4:57-61.

Even when the display is black, some light will leak through the display. 1:57-61. The amount of light that leaks through the display can increase as the viewer changes the angle at which they view the display. 1:61-2:3. One way to reduce light leakage is to add what is known as a C-plate optical compensator. 5:49-62. While C-plate optical compensators can improve contrast, they do not improve another key feature of LCD displays – gray scale stability. 5:65-66. For example, at certain gray scale voltage levels the display may appear black while viewing at one angle and white at another viewing angle. 7:1-5. O-plate optical compensators can be used to provide improved gray scale stability. 7:8-10.

The compensators are birefringent materials. 7:8-15; 7:33-35. There are two types of birefringent materials, uniaxial and biaxial. A uniaxial material has one unique index of refraction along an axis, referred to as the extraordinary axis, that is different from the other indices along axes perpendicular to the extraordinary axis. 2:61-3:1. If the unique index is larger than the other indices the material is referred to as positively birefringent. 3:2-4. If the unique index is lower the material is negatively birefringent. 3:4-6. A biaxial birefringent material has three different indices of refraction, along three different axes that are perpendicular to each other. 3:9-14. The axis with the largest index of refraction is referred to as the principal optic axis. *Id.* The patent uses a term “optical symmetry axis” to refer to both the extraordinary axis of uniaxial material and the principal optic axis of a biaxial material. 3:14-17.

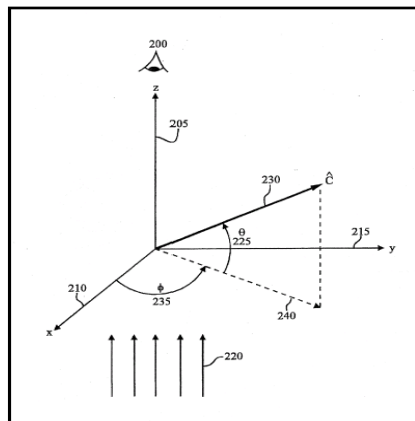


Figure 2 of the ‘352 patent, above, shows an optic axis designated as 230 within an x-y-z three dimensional coordinate system. The viewer (eyeball in figure) looks down the z-axis. A tilt angle θ is defined as the angle between the optic axis and the x-y plane. 3:51-59.

The ‘352 patent discloses and claims a compensator that has a varying tilt angle. 10:64-11:5. Such a compensator improves the contrast ratio and gray scale stability over a wide range of viewing angles. 10:51-55.

a. A layer of a birefringent material (Claim 3) (JCC Ex. R, p. 1)

The specification of the ‘352 patent provides the following definition of what is a birefringent material:

“Many of the materials disclosed in this document are birefringent. That is to say, they have varying indices of refraction depending on the direction of the electric vector of the light propagating through the material. The index of refraction is the ratio of the speed of light in a vacuum to that in the material.” 2:53-58.

CMO’s proposed construction for a layer of a birefringent material: “a layer of material

that has varying indices of refraction depending on the direction light travels through the material. An index of refraction is the ratio of the speed of light in a medium relative to the speed of light in a vacuum” tracks the specification nearly verbatim, replacing the technical phrase “direction of the electric vector of the light propagating through the material” with the more familiar phrase “direction light travels through the material.”

The ‘352 patent describes two types of birefringent material, uniaxial and biaxial. 2:53-3:14. Within the uniaxial family there are positively birefringent materials and negatively birefringent material. LGD attempts to limit the term birefringent to only positively birefringent uniaxial materials. Limiting the claims to such a narrow choice of materials is completely contrary to the teaching of the patent: “[i]n general, O-plate compensators may also include A-plates and/or *negative* C-plates as well as O-plates.” 12:60-61 (emphasis added); *see also* 10:44-45 (“It is the goal of this invention to provide a process for producing O-plates which have the desired biaxial symmetry ...”). The patent contemplates use of compensators with birefringent materials that are negative and biaxial in nature. LGD’s attempt to unduly limit the construction of birefringent material to positive and uniaxial should be rejected in view of the direct teachings of the ‘352 patent.

b. Optical symmetry axis (Claim 3) (JCC Ex. R, p. 1)

The meaning of the term “optical symmetry axis” as used in the ‘352 patent is unequivocal:

“In this document the term “optical symmetry axis” will be defined to mean the extraordinary axis in uniaxial materials and the principal optic axis in biaxial materials.” 3:14-17

As clearly stated in the ‘352 patent, the construction of “optical symmetry axis” must allow the trier of fact to identify this axis in both uniaxial and biaxial materials, which CMO’s construction does: “the extraordinary optic axis in uniaxial materials and the principal optic axis in biaxial materials. A uniaxial material has two axes with the same index of refraction and another axis, the extraordinary axis, that has a different index of refraction. A biaxial material

has three axes each with a different index of refraction, and the axis with the highest index of refraction is the principal optic axis.”

LGD’s construction attempts to narrow the definition to uniaxial material by proposing a construction that includes only the extraordinary axis. This construction contradicts the stated definition in the specification which expressly states that the principal optic axis of a biaxial material is an “optical symmetry axis.”

c. Tilt angle varies along an axis normal to said layer (Claim 3) (JCC Ex. R, p. 2)

The heart of the dispute for this term is LGD’s attempt to limit the variation in tilt angle to be between 25° and 65°. It is well settled that a claim should not be construed to exclude an embodiment of the invention, unless specifically disclaimed. *Oatey Co. v. IPS Corp.*, 514 F.3d 1271, 1276-77 (Fed. Cir. 2008). The patent specification discloses a compensator with a tilt angle that can range between 20° to 80°: “[t]he O-plate layer 1100 comprises birefringent liquid crystal polymer layer having an optical symmetry axis 1120 oriented, on average , at a tilt angle 1125, relative to the surface of the liquid crystal polymer layer 1110, of approximately 20° to 80°.” 12:45-49. An adoption of LGDs construction that limits the tilt angle to a range of 25° to 65° would therefore exclude an embodiment of the invention.

Additionally, claim 1 of the patent expressly recites a tilt angle range between 25° to 65°. *See* Claim 1. If the patentee intended to include such a limitation in claim 3 it certainly knew how to do so. In contrast, the asserted claims merely require a varying tilt angle. The claims should not be construed to limit the tilt angles to a specified range.

d. A desired viewing characteristic over a specified field of view (Claim 29) (JCC Ex. R, p. 2)

LGD contends that the term “a desired viewing characteristic over a specified field of view” is indefinite. It is well known in the art that LCD displays have product specifications that list the viewing angle as a function of contrast ratio. Yeh Decl. ¶¶ 7-10. The contrast ratio is a luminance at a bright state divided by a luminance at a dark state. *Id.* CMO’s construction reflects this basic understanding in the art.

2. U.S. Patent No. 6,008,786 (JCC Ex. S)

The '786 patent discloses a method and device for correcting the color of a LCD for differences in the amount of light transmitted (transmissivity) through the display for different colors. 3:12-31. Each color displayed on an LCD is made up of a combination of primary colors, typically red, green, and blue (often referred to as R/G/B). Each of these colors has its own set of pixels in an LCD. Different colors are displayed by varying the amount of voltage sent to the pixels representing each of the primary colors. By adjusting the amount of red, green, and blue light transmitted, the LCD can display a full range of color. 2:33-36. In order to display the range of colors, it is important to be able to vary the amount of voltage provided to each pixel; they are not simply turned on or off. 1:47-52. The different levels of voltage are referred to as "gray scales."

Ideally, the relationship between gray scale, applied voltage, and transmissivity is the same for each of the R/G/B colors. However in practice, the gray scale and the achieved transmissivity have a slight difference depending on color. 1:66-2:2. To address this problem, the '786 patent describes a computing circuit for performing an addition or subtraction of the gray scale signal for at least one color to generate a corrected gray scale signal. 3:27-29. The corrected gray scale signal for one color is corrected for the color dependent difference in transmissivity relative to the gray scale signal for another color, which is uncorrected for the color dependent difference in transmissivity. 4:31-37. The uncorrected gray scale signal is also delayed while the gray scale signal of the one color is being corrected, so that the gray scale signals are properly synchronized for display. 2:1-19; 5:23-30.

a. Driver means (Claim 1) (JCC Ex. S, p. 1)

The parties agree that this term should be interpreted pursuant to 35 U.S.C. § 112 ¶ 6. CMO contends that the claimed function has its plain and ordinary meaning - "driving the display cell with grey scale data signals." LGD argues that the claimed function is "driving the display cell with sets of grey scale data signals," which improperly adds the requirement of "sets." The parties generally agree that the corresponding structure includes X-driver 3 (Fig. 1),

but LGD tries to exclude any equivalents to this structure. Section 112, however, expressly includes within the scope of means-plus-function claims “the corresponding structure, material, or acts described in the specification *and equivalents thereof*.” 35 U.S.C. § 112 ¶ 6 (emphasis added). The proper claimed function is “driving the display cell with grey scale data signals,” and the appropriate corresponding structure is X-driver 3 (Fig. 1) and equivalents.

b. Data control means (Claim 1) (JCC Ex. S, p. 1)

The parties agree that this term should be interpreted pursuant to 35 U.S.C. § 112 ¶ 6, and that the claimed function is “receiving gray scale data signals related to the setting of a gray scale for the display cell and outputting said gray scale data signals to said driver with a predetermined timing.” LGD argues that the corresponding structure is Fig. 5, all elements; Figs 6-8. LGD’s construction ignores other embodiments disclosed in the specification that are not the “Preferred Embodiment.” This is error. *Micro Chem., Inc. v. Great Plains Chem. Co., Inc.*, 194 F.3d 1250, 1258 (Fed. Cir. 1999). While the ‘786 patent primarily contains preferred embodiments, *see, e.g.*, 3:62-65 (“PREFERRED EMBODIMENT – The subject invention *can be* realized”), the patent explains and describes other embodiments that also practice the claimed invention. *See, e.g.*, 6:1-9 (“[I]t should be understood that many changes can be made in the described embodiment without departing from the spirit and scope of the present invention.”). Indeed, the claim itself states that the “data control means” includes both computing means and buffer means. 6:20-31. *See also* 3:25-31 (“Summary of the Invention” stating that “the data control means includes a computing circuit” and “*also* includes delay means”). The appropriate corresponding structure is computing circuit 32, buffer circuit 26, delay circuit 24 (Fig. 5) and equivalents. The buffer means appropriately includes both the circuitry relating to the delay and the buffer circuitry where the gray scale data signal is temporarily stored for the time of the delay. 5:23-30.

c. Computing means (Claim 1) (JCC Ex. S, p. 2)

The parties agree that this term should be interpreted pursuant to 35 U.S.C. § 112 ¶ 6, and

that the claimed function is “changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium.” LGD argues that the corresponding structure is Fig. 5, elements 32, 33, 34; Figs. 6-8. LGD is thus attempting, improperly, to add structure to the claim construction that is not required to perform the claimed function. *Asyst Techs., Inc. v. Empak, Inc.*, 268 F.3d 1364, 1370 (Fed. Cir. 2001). The specification explains that “[w]ith the method of the subject invention, *only* an additional circuit such as a computing circuit, is needed to effectively correct the differences in the transmissivity/applied voltage characteristics for the colors.” 5:58-61; *see also* 4:31-37; 3:25-31. Furthermore, the specification discloses alternative embodiments to the preferred embodiment in figure 5, including software and hardware equivalents. *See, e.g.*, 4:55-57. The proper corresponding structure is computing circuit 32 (Fig. 5) and equivalents.

- d. Changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level (Claim 1) (JCC Ex. S, p. 2)/Changing the level of gray scale data signals related to at least one of the multicolors supplied to the display cell to create a corrected gray scale data signal with a level different from the inputted gray scale data signal (Claim 5) (JCC Ex. S, p. 5)/Changing the gray scale data signals related to one of the multicolors (Claim 12) (JCC Ex. S, p. 10)**

CMO contends that these limitations are unambiguous. The “changing” language of claim 1 is already included in the construction of “computing means,” and further construction is unnecessary and improperly repetitive. Should the Court decide that the other terms require construction, CMO proposes the modestly simplified constructions provided in the JCC, which remove unnecessary wording.

LGD argues that these terms means “adding or subtracting compensation values to modify the gray scale levels of one or more, but not all, color video signals.” But this violates basic principles of claim differentiation because dependent claim 4 adds this limitation of addition or subtraction. 6:40-43. The specification discloses that “the data control means includes a computing circuit for performing an addition or subtraction of the gray scale” (3:26-

29), not just adding or subtracting compensation values to modify the gray scale levels as LGD would require. Also, LGD's addition of the term "color video signals" lacks support in the specification and adds ambiguity to the otherwise clear claim language.

e. Buffer means (Claim 1) (JCC Ex. S, p. 3)

"Buffer means" recites sufficient structure – a buffer – to remove the term from the ambit of 35 U.S.C. §112 ¶6. To invoke this statute, the alleged means-plus-function claim element may not recite a definite structure which performs the described function. Thus, just because a named element of a patent claim uses the word "means" does not make that element a "means-plus-function" element under 35 U.S.C. § 112 ¶ 6. *Cole v. Kimberly-Clark Corp.*, 102 F.3d 524, 531 (Fed. Cir. 1996). Here, the term at issue recites a specific structure – a buffer – to perform the described function of delaying an uncorrected gray scale signal for the time delay caused by correcting another gray scale data signal. The plain and ordinary meaning of "buffer" should apply, or alternatively, if the Court determines construction is necessary, "buffer means" means "memory where gray scale data signals can be temporarily stored and delayed."

If the Court determines that this term should be interpreted pursuant to 35 U.S.C. § 112 ¶ 6, the parties agree that the claimed function is "delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected." LGD argues that the corresponding structure is Fig. 5, element 24, but this improperly omits the necessary corresponding structure of the buffer circuit 26 (Fig. 5) and equivalents. The claim term "buffer means" naturally includes a buffer circuit. As the specification explains, the delay circuit 24 works in conjunction with the buffer circuit 26 to synchronize the gray scale data signals. 5:23-30.

- f. Delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected (Claim 1) (JCC Ex. S, p. 4)/Delaying the output for at least one other of the multicolor by the time taken for correction of said at least one color (Claim 5) (JCC Ex. S, p. 6)/Delaying the gray scale signals for the other of the colors (Claim 7) (JCC Ex. S, p. 9)/Delaying the output for any other color of the multicolors with gray scale data signals not subject to a correction by the amount of time taken for correction of the one color (Claim 12) (JCC Ex. S, p. 11)**

CMO contends that these limitations are unambiguous. The “delaying” language of claim 1 is already included in the construction of “buffer means,” and further construction is unnecessary and improperly repetitive. Should the Court decide that the other terms require construction, CMO proposes the modestly simplified constructions provided in the JCC, which remove unnecessary wording.

LGD argues that these “delaying” clauses require “holding or deferring at least one color video signal that is not subjected to a compensation value by the amount of time taken to modify another color video signal.” LGD’s addition of the terms “holding or deferring” and “color video signals” lacks support in the specification and adds ambiguity to the otherwise clear claim language. Also, LGD’s requirement of a “not subjected to a compensation value ... to modify another color video signal” is improper because the specification discloses that “the data control means includes a computing circuit for performing an addition or subtraction of the gray scale” (3:26-29), not just adding or subtracting compensation values to modify the gray scale levels as LGD would require.

- g. Adjusting means (Claims 2, 3) (JCC Ex. S, pp. 4-5)**

The parties agree that this term should be interpreted pursuant to 35 U.S.C. § 112 ¶ 6, and that the claimed function regarding claim 2 is “varying the amount of correction accorded to the gray scale data signals for said at least one color.” LGD argues that the corresponding structure is Fig. 5, elements 33, 34; Figs. 6-8, but this is unnecessarily over inclusive. The specification discloses that only an additional circuit, such as a computing circuit, is needed to effectively correct the differences in transmissivity (which includes varying the amount of adjustment with the grey scale level). 5:56-60. The appropriate corresponding structure is thus computing circuit

32 (Fig. 5) and equivalents.

Regarding the “adjusting means” of claim 3, the claim states that the adjusting means assists the data control means to simultaneously output the corrected and uncorrected gray scale data signals, which relates to the “buffer means” portion of the data control means. The claimed function is the same as for the buffer means – “delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected.” The corresponding structure is buffer circuit 26, delay circuit 24 (Fig. 5) and equivalents. *See* 5:23-30. LGD argues that this is indefinite, but one of ordinary skill in the art would understand that claim 3 should depend from claim 2 and the “adjusting means” of claim 2 provides the antecedent basis for the same term in claim 3. Villasenor Decl. ¶ 13.

h. Simultaneously output the gray scale data of all said multicolors (Claim 5) (JCC Ex. S, p. 7)/Synchronize the timing of the gray scale data signals for all said multicolors (Claim 12) (JCC Ex. S, p. 11)

CMO contends that these limitations are unambiguous. To the extent that the Court determines construction is necessary, the “simultaneously output ...” language of claim 5 means “outputting the gray scale data of all the multicolors from a buffer at about the same time.” The specification uses the terms “simultaneous” and “synchronized” in the same context of providing to the driver circuitry the uncorrected gray scale data at about the same time as the correct gray scale data to compensate for the small difference in processing time. 3:29-31; 5:23-30; 4:11-18. As stated in the claim 5, “synchronized” is the result of “simultaneous” output. Claim 5 (“synchronizing the output of the gray scale data signals by delaying ... to simultaneously output the gray scale data of all said multicolors”).

LGD argues that both of these claim phrases mean the same thing – “provides all multicolor gray scale data to the data driver during the same predetermined time interval.” This is incorrect because it improperly attempts to import the term “predetermined” into these limitations. In addition, the term “time interval” lacks support in the specification and adds ambiguity to the otherwise clear claim language. Also, LGD’s proposed construction improperly

equates “simultaneously output” with “synchronize.” The plain meanings of the phrases are clear and should apply.

i. Display cells (Claim 7) (JCC Ex. S, p. 7)

CMO contends that the plain meaning of “display cells” should apply. LGD argues that “display cells” is indefinite. One of ordinary skill in the art understands the term “display cells” in the context of the ‘786 patent. Villasenor Decl. ¶ 14.

j. Calculation logic [in the driver circuit of at least one color] for changing the level of the gray scale data signals of said at least one color to a different gray scale level (Claim 7) (JCC Ex. S, p. 8)/Driver circuit for any other of the colors without the calculation logic in its driver circuit (Claim 7) (JCC Ex. S, p. 8)/Said data control means [includes an addition or subtraction of the binary signal representing a change of at least one gray scale level for at least one color] (Claim 11) (JCC Ex. S, p. 9)

CMO contends that the plain and ordinary meaning for the “calculation logic ...” phrase should apply, or alternatively, if the Court determines construction is necessary, it means “structure, including a driver circuit, that changes the gray scale data signal for at least one color relative to the other colors.” The specification describes reducing the gray scale data for blue in comparison with the gray scale data for red and green. 4:31-37. The specification further explains that this reduction can be done by either software or hardware. 4:55-57.

LGD argues that “calculation logic ...” means “calculation logic ... for adding or subtracting compensation values to modify one or more, but not all, color video signals.” LGD’s proposed construction violates principles of claim differentiation because dependent claim 11 adds the same limitation of adding or subtracting. 8:3. Moreover, the specification discloses that the present invention includes “performing an addition or subtraction of the gray scale” (3:26-27), not just adding or subtracting *compensation values* to modify color video signals as LGD would require. Also, LGD’s addition of the term “color video signals” lacks support in the specification and adds ambiguity to the otherwise clear claim language.

CMO contends that the related phrase in claim 7 “driver circuit for any other of the colors without the calculation logic in its driver circuit” is unambiguous. LGD argues that the phrase

should be construed as “at least one color video signal path that does not include calculation logic.” LGD’s proposed construction is incorrect because LGD’s addition of the term “color video signal path” lacks support in the specification and adds ambiguity to the otherwise clear claim language.

LGD argues that “said data control means” in claim 11 is indefinite. In the context of the claims and the rest of the ‘786 patent, one of skill in the art would understand this to be referring to the “calculation logic” term of the immediately preceding claim 10 from which claim 11 depends. In that context, the term means “structure that can add or subtract a binary signal representing a change of at least one gray scale level for at least one color.” Villasenor Decl. ¶ 15.

3. U.S. Patent No. 6,013,923 (JCC Ex. T)

The ‘923 patent discloses a method of protecting a semiconductor switch array, like the TFT switch array of an LCD panel, from electrostatic discharge (“ESD”) damage. 1:7-10. As discussed above, ESD is the slight shock one feels immediately before one touches a metal doorknob after walking across a carpet. This can damage the tiny transistors of an LCD panel. 1:20-24. The ‘923 patent addresses this problem and provides protection against ESD during fabrication of the TFT switch array during testing or when connecting peripheral circuits to the LCD panel. 5:33-35.

The ‘923 patent describes connecting the TFT array both directly and through protection elements to shorting elements, which are themselves connected. 3:54-62; 8:11-18. These connections provide current paths for leaking the electrostatic charges that collect on the gate and source lines to ground. 5:60-64. Because the shorting bars connect the gate and source electrodes of all of the TFT switches in the array, the gate and source electrodes remain at the same potential throughout the fabrication process, which prevents any voltage differentials from occurring across the gate and source electrodes. This inhibits ESD damage. 1:64-2:3.

a. Source line (Claim 1) (JCC Ex. T, p. 1)

CMO contends that the plain and ordinary meaning of “source line” is appropriate, or, if the Court determines that construction is necessary, “source line” means “conductor that connects the source terminals of pixel transistors and leads to the source amplifiers.” As one of ordinary skill in the art would understand, a transistor has three terminals, one of which is called the “source.” *See, e.g.,* Ex. T-2 (IEEE Standard Dictionary of Electrical and Electronics Terms at 403 (defining “field-effect transistor”)). The specification explains that source lines “interconnect the pixels of each column” and “lead to charge amplifiers.” 4:65-66; 5:1-3.

LGD argues that “source line” means “a pattern of electrically conductive material that conveys data signals to transistors within the TFT array.” This construction is incorrect because it is overbroad. With LGD’s definition, a “source line” could be any conductive material that conveys any signal to the TFTs, not just the signal appropriate for the source terminal of the TFT. In addition, in the context of this patent, it is more accurate to define the source lines by what they connect as described by the specification, not by a possible use. Also, LGD’s construction improperly adds limitations to the claims. For example, there is no support that a “source line” must be a “pattern.” As another example, adopting LGD’s phrase “*within* the TFT array” would erroneously exclude the preferred embodiment, which describes the source lines as extending *beyond* the TFT array to the shorting element and a portion of the source lines is cut off with the shorting element before testing. 7:32-40.

b. Gate line (Claim 1) (JCC Ex. T, p. 1)

CMO contends that the plain and ordinary meaning of “gate line” is appropriate, or, if the Court determines that construction is necessary, “gate line” means “conductor that connects the gate terminals of pixel transistors and leads to the gate driver circuit.” As one of ordinary skill in the art would understand, a transistor has three terminals, one of which is called the “gate.” *See, e.g.,* Ex. T-2 (IEEE Standard Dictionary of Electrical and Electronics Terms at 403 (defining “field-effect transistor”)). The specification further explains that gate lines “interconnect the pixels 22 of each row” and “lead to a gate driver circuit.” 4:64-65; 4:66-67.

LGD argues that “gate line” means “a pattern of electrically conductive material that conveys gate signals to transistors within the TFT array.” This construction is incorrect because in the context of this patent, it is more accurate to define the gate lines by what they connect as described by the specification, not by a possible use. In addition, LGD’s construction improperly adds limitations to the claims, as previously explained for its similarly flawed construction for “source line.”

c. During formation of said gate lines (Claim 1) (JCC Ex. T, p. 2)

The claim phrase “during formation of said gate lines” means “during the manufacturing stages in which the gate lines are formed and connected.” Claim 1 requires that during formation of said gate lines, one end of each gate line is connected directly to a shorting element and another end of each gate line is connected to a shorting element via a protection element. 8:11-14.

LGD argues that “during formation of said gate lines” means “at the same time when the electrically conductive material that forms the gate lines is deposited and etched,” but this limited view would exclude the preferred embodiment. The specification explains that the protection element includes a metal connection tab contacting the gate line through a via. 7:22-31. As one of skill in the art would understand, a via is a path filled with conducting material between circuit layers. *See, e.g.*, Ex. T-3 (Integrated Circuit Engineering Corporation, Practical Integrated Circuit Fabrication at 16-18 (1984)). In the embodiment described in the specification and shown in Fig. 9, formation of the gate lines includes the processing steps in which the gate line 124 is connected to shorting element 156 with the protection element 170, 178 through the via 172. 7:22-31. Accordingly, “during formation ...” cannot be limited to the time at which gate line 124 was deposited and etched – it must include subsequent formation steps necessary to make the connections between the gate line and the shorting elements.

The specification states that “ESD damage protection circuits are present from the first manufacturing stage of the TFT switch array (gate line formation).” 7:49-51. This further

supports CMO's construction because the ESD protection circuit is not present until the connection is made from the gate line to the shorting element and the circuit is completed. The context of the patent further emphasizes that the focus is on the connections between the gate (and source) lines and the shorting elements (5:41-64), and that one of skill in the art would appreciate that variations and modifications may be made to the invention without departing from the scope thereof as defined by the claims. 7:66-8:2.

d. Shorting element (Claim 1) (JCC Ex. T, p. 2)

"Shorting element" is unambiguous. LGD, however, argues that it means "a pattern of conductive material for electrically connecting, with low resistance, the gate lines to each other or the source lines to each other." This is incorrect because LGD erroneously introduces new limiting language including "a pattern of." In addition, LGD improperly adds the concept of "low resistance," which confuses this term in the context of the patent with the separate term "resistive protection element."

e. Protection element (Claim 1) (JCC Ex. T, p. 3)

CMO contends that "protection element" means "element protecting from electrostatic discharge (ESD)." This is supported by the claim language itself and the context of the patent. The specification explains that protection elements provide current paths for leaking electrostatic charges collected by the gate and source lines (5:60-62), and provides several concrete examples, including "TFT switches, TFD's (thin film diodes), zener diodes or photodiodes." 6:12-13. All of these elements protect from ESD by conducting current to ground and preventing build-up of a harmful voltage differential.

LGD argues that "protection element" means a "circuit component designed to protect against electrostatic discharge and to allow for testing," but this is incorrect. LGD again attempts to introduce new limitations, for example, "designed to" and "to allow for testing," in its proposed construction. The vague, additional language does not help to define the appropriate scope of the patent.

f. During formation of said source lines (Claim 1) (JCC Ex. T, p. 3)

CMO contends that “during formation of said source lines” means “during the manufacturing stages in which the source lines are formed and connected.” Claim 1 requires that during formation of the source lines, one end of each source line is connected directly to a shorting element and the other end of each source line is connected to a shorting element via a protection element. 8:15-18.

LGD argues that “during formation of said source lines” means “at the same time when the electrically conductive material that forms the source lines is deposited and etched.” LGD’s construction here is wrong for the same reasons as its proposed construction of “during formation of said gate lines.” Specifically, LGD seeks to exclude the preferred embodiment. The specification explains that the protection element includes a metal connection tab contacting the gate line through a via. 7:22-31. One of skill in the art would understand “during formation ...” can not be limited to the time at which gate line 124 was deposited and etched – it must include subsequent formation steps necessary to make the connection between the gate line and the shorting element. The specification expressly states that both sets of resistive protection elements 154 (for gate lines) and 158 (for source lines) are similar, and thus, the same understanding applies equally to “during formation of said source lines.” In addition, the context of the patent further emphasizes that the focus is on the connections between the source (and gate) lines and the shorting elements (5:41-64), and that one of skill in the art would appreciate that variations and modifications may be made to the invention without departing from the scope thereof as defined by the claims. 7:66-8:2.

g. Electrically coupling said shorting elements (Claim 1) (JCC Ex. T, p. 4)

CMO contends that “electrically coupling said shorting elements” means “electrically connecting the shorting elements.” The specification explains that the shorting rings are “electrically connected” through vias formed in the TFT switch array structure. 5:57-64.

LGD argues that the term means “electrically connecting the shorting elements without intervening protection elements.” LGD’s proposed construction is incorrect because it attempts

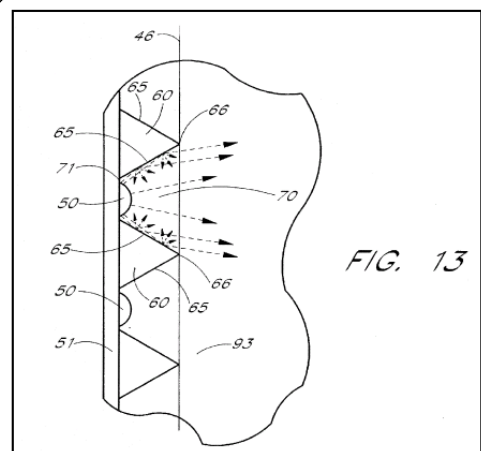
to add a limitation to the claims – “without intervening protection elements.” Importing limitations from the specification to the claims like this would be error and must be rejected.

4. U.S. Patent No. 6,134,092 (JCC Ex. U)

The ‘092 patent discloses a device that can illuminate a display such as an LCD. 2:60-64. For LCDs it is important for the illumination device to provide a substantially uniform distribution of light across the display area. 1:17-18. In prior art devices light tends to decrease in intensity away from the light sources resulting in bright spots around the edge of the display. 1:18-23. The illumination device disclosed in the ‘092 patent includes a plurality of guide members that facilitate a more uniform distribution of light. The illumination device includes a plurality of point light sources, such as LEDs, that inject light into a waveguide. 3:18-22. The waveguide is located adjacent to a light guide that has a plurality of spaced apart guide members. 3:42-47. The guide members extend from a planar member of the light guide. *Id.* A cover is located over a periphery of the waveguide and includes an aperture that emits light. 6:66-7:2;7:36-39. The guide members, planar member and inner surface of the cover all have diffusive reflective surfaces. 4:24-26; 6:2-5. The diffusive reflective surfaces of the guide members, planar member and cover form optical cavities that inject light into a side surface of the waveguide. 7:5-12. The guide members have angled side surfaces that reflect light into the waveguide in areas between the light sources to create a relatively uniform distribution of light in the peripheral portion. 7:22-26.

a. Peripheral portion (Claims 1, 12) (JCC Ex. U, p. 1)

CMO’s construction for peripheral portion is “a portion of the waveguide that is covered by a cover”, which construes this claim language in terms of an area of the waveguide. LGD’s construction “boundary adjacent a side edge”, limits the peripheral portion to an edge of the waveguide. LGD’s construction is inconsistent with the



specification and other relevant language of the claims.

The patent discusses a uniform distribution of light in the “peripheral portion” of the waveguide. 7:12-15; 7:23-26. If the peripheral portion is the edge, then the edge of the waveguide would have to be substantially uniformly illuminated. But this is contrary to the teachings of the specification. Fig. 13 from the ‘092 patent shows a series of triangular shaped guide members 60 that each have reflective surfaces 65. Each guide member has an apex 66 that intersects the edge of the waveguide 46. Because the apexes are in contact with the waveguide edge 46, very little, if any light will travel into those portions of the edge. Yeh Decl. ¶¶ 12-15. The result would not be uniform light distribution along the edge – as required by LGD’s proposed construction – but a series of dark(er) spots at the apexes of each guide member. *Id.*

Additionally, item 93 is identified as the peripheral portion of the waveguide. 7:26. The designation 93 clearly does not point to the edge of the waveguide but to an area inward from the edge.

Construing peripheral portion as an edge is also inconsistent with claim 25. Claim 25 recites a peripheral edge. The fact that the claims include recitations to both peripheral portion and peripheral edge strongly suggest that these terms cover different structures of the device.

LGD’s construction limiting the peripheral portion to an edge should be rejected in favor of CMO’s definition which construes peripheral portion to mean the area of the waveguide beneath the cover, as explained in the patent: “[t]he cover 48 (shown in phantom lines) is mounted over the periphery of the waveguide 46 with the aperture 82 preferably aligned midway between the apexes 66a and 66b.” 6:66-7:2.

b. A series of point light sources (Claim 1) (JCC Ex. U, p. 1)

CMO contends that this term is unambiguous. LGD not only believes the term needs construing but proposes a construction that imports unnecessary limitations. LGD’s construction “a sequence of separate components, such as light-emitting diodes, that provide the desired light that illuminates the waveguide or optical cavity,” requires that the light sources be “separate”

components and adds a function, providing a desired light to illuminate the waveguide or optical cavity. This improper importation of limitations should be rejected. To the extent the Court construe's this term then CMO's construction of "three or more solid state light sources" should be adopted. *See* 1:27-34; 3:18-22.

c. Diffusive reflective surfaces/Diffusive reflective optical cavities (Claims 1, 12, 17, 21) (JCC Ex. U, p. 2 & 6)

CMO submits that these terms need no construction. A diffusive reflective surface is a surface that diffusively reflects light. Likewise, a diffusive reflective optical cavity is a space between surfaces (a cavity) that diffusively reflect light. LGD agrees that the surfaces reflect and diffuse (scatter) light, but tries to add another requirement that the surface must be non-transparent. There is nothing in the record to indicate that the diffusive reflective surfaces be non-transparent.

To the extent these terms need to be construed then CMO request the adoption of its construction for diffusive reflective surfaces to mean "surfaces, including a surface that extends upward relative to a planar surface, that diffusively reflect light" and diffusive reflective optical cavities to mean "a space between diffusive reflective surfaces." The requirement that at least one surface extend from a planar surface is inherent from the specification and the claims. For example, claim 12 recites a series of diffusive reflective optical cavities formed by diffusive reflective surfaces. As disclosed in the specification an optical cavity is formed by four surfaces, the planar member, cover and two guide member surfaces. 7:5-12. The side surfaces, or guide members, extend from the planar surfaces. 3:44-47. The extension of the side surfaces is required to create the optical cavities and is thus inherent in the claims.

These terms should be given their plain and ordinary meaning, and if not, then CMO's constructions should be adopted.

d. The diffusive reflective surfaces oriented relative to the series of point light sources and the waveguide so as to introduce light in regions of said waveguide between pairs of said point light sources (Claim 1) (JCC Ex. U, p. 3)

The primary difference between the parties constructions relates to the orientation of the

diffusive reflective surfaces. CMO's construction follows the teaching of the '092 patent, which provides that the tapered or angled surfaces reflect light into the regions between light sources. LGD's construction, on the other hand, lacks clear support from the '092 patent.

The '092 patent explains that, in order to provide light to the areas between light sources (LEDs), the invention uses tapered or angled side surfaces to reflect light into the waveguide:

"The angled side surfaces 65 reflect the light rays into the waveguide 46. This reflected light fills the regions between adjacent LEDs 50 to thereby provide a relatively uniform distribution of light injection from the LED 50 into the peripheral portion of the waveguide 46." 7:22-26.

CMO's construction accurately reflects this structure: "the diffusive reflective surfaces are angled relative to each other to direct light from the point light sources into the waveguide." LGD's proposed construction, which involves a complicated description of the orientation of the surfaces, is not supported by the specification. The Court should thus adopt this CMO's proposed construction.

e. Light-emitting diodes mounted on an electrical-conductive strip of material (Claim 5) (JCC Ex. U, p. 4)

This term is clear and unambiguous. The meaning of light-emitting diode is well known to those skilled in the art. Yeh Decl. ¶ 16. The other part of this term is self-described. A strip of material that is electrically conductive. LGD's construction attempts to narrow the definition of LED to a component that contains a semiconductor diode chip and the function of providing a desired light to illuminate the waveguide or optical cavity. These added definitions are both unnecessary and not supported by the intrinsic record.

f. Guide members positioned along a periphery of the optical cavity (Claim 21) (JCC Ex. U, p. 6)

CMO submits that this term be given its plain and ordinary meaning or in the alternative be construed to mean "guide members are spaced apart along a side of the optical cavity." LGD attempts to graft an additional requirement into the claim: that the guide members be separate structures unattached to one another. This additional requirement is contrary to the

embodiment disclosed in the specification. The specification shows that the guide members extend from and are attached to each other by the planar member. 3:42-47; Figs. 2 and 4. Consequently, LGD's construction should be rejected.

g. Whereby the peripheral portion of the waveguide is substantially uniformly illuminated (Claim 1) (JCC Ex. U, p. 4)

A "whereby" clause that merely states the result of the limitations of the claim is not a claim limitation. *Lockheed Martin Corp. v. Space Sys./Loral, Inc.*, 324 F.3d 1308 (Fed. Cir. 2003). The language preceding the whereby clause in claim 1 recites a series of diffusive reflective surfaces that are oriented relative to a series of point light sources and the waveguide so as to introduce light into regions of the waveguide between pairs of light sources. As stated in the '092 specification, the angular orientation of the diffusive reflective surface causes the substantially uniform distribution of light within the peripheral portion of the waveguide: "[t]his reflected light fills the regions between adjacent LEDs 50 to thereby provide a relatively uniform distribution of light injection from the LED 50 into the peripheral portion 93 of the waveguide." 7:23-26. The orientation of the diffusive reflective surfaces introduce light into regions of the waveguide between light sources and create a substantially uniform distribution of light. The whereby clause explains the result of using this structure – it is therefore not a claim limitation. If the clause were a claim limitation then it should be construed in accordance with CMO's construction of peripheral portion.

h. Whereby light is injected from said exit mouths into a peripheral portion of said optical cavity (Claim 17) (JCC Ex. U, p. 7)

The language preceding the whereby clause in claim 17 recites a series of diffusive reflective optical cavities that each have an exit mouth and a series of point sources of light that emit light into the optical cavities. Light that goes into a cavity will, of course, come out of the cavity and into the waveguide. 7:16-30; Fig. 13. The whereby clause recited in claim 17 thus merely describes the result of injecting light into the optical cavities. The whereby clause should therefore not be construed as a claim limitation. If the clause were a claim limitation, it should

be construed in accordance with CMO's constructions of exit mouth and peripheral portion.

5. U.S. Patent No. 6,734,926 (JCC Ex. V)

The '926 patent describes a method of narrowing a liquid crystal display by mounting certain control circuitry on the side of the display as opposed to the rear of the display. 1:6-11. LCD screens include a reflecting plate for reflecting light from a light source through the liquid crystal material and out to the viewer. 1:40-53. Control circuitry, mounted on the back of the reflecting plate, receives "signals sent from an imaging device such as a computer video card" and "generates corresponding signals for [an] X-board [and] Y-board [which in turn] generate corresponding control signals for the LCD panel ... to display images." 1:61-67; Fig. 2. By moving this control circuitry from the back of the reflecting plate to other positions on the sides of the display panel, the patentees were able to narrow the thickness of the display panel and reduce production cost. 8:24-27.

- a. Display apparatus (Claims 1, 2, 5, 8, 9, 12, 15, 16, 19, 22, 23, 26, 29, 30, 33, 36, 37, 40) (JCC Ex. V, p. 1)/Upper Frame (Claims 1, 8, 15, 22, 29, 36) (JCC Ex. V, p. 1)/An array of light tubes disposed behind the display panel (Claims 1, 8, 15, 22, 29, 36) (JCC Ex. V, p. 1)**

These terms should be given their plain and ordinary meaning. LGD, however, proposes substituting the term "display *product*" for "display *apparatus*." This does nothing to clarify the meaning of the term. Regarding "upper frame," LGD improperly seeks to add a limitation that it must be the "outermost front cover." This is not supported by the '926 specification, which requires only that the upper frame "protect[s] internal components" and "hold[s] in place the internal components of the LCD monitor." Abstract, 1:40-44. Regarding the array of light tubes, LGD seeks to limit the term improperly to "fluorescent lamps" "along the back" of a "direct type backlight unit." But no mention is made in the claims or the '926 specification of the invention being limited to use with florescent lamps, as LGD urges. Moreover, while the preferred embodiments in the '926 patent describe a direct-type LCD, the specification notes that "[t]hose skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above

disclosure should be construed as limited only by the metes and bounds of the appended claims.”

8:28-33. There is no reason that the invention cannot be applied to non-direct type LCDs. Finally, the claim states that array is “behind the display panel”—not “along the back” of the backlight unit as LGD suggests.

b. Being separated from the side portion [of the supporting plate] by a gap” (Claims 1, 8) (JCC Ex. V, pp. 2-3)

This language does not need construction. If construed, CMO’s construction is preferable as LGD’s proposed construction requires that there be a space “bounded by a sub-frame and a side portion,” insinuating that nothing else can be located between the sub-frame and side portion. That is not a limitation of the invention described in the ‘926 patent.

c. A circuit board installed [within the gap/on the side portion of the reflecting plate/on the side portion of the supporting plate/at least one of the side portions of the reflecting plate/at least one of the side portions of the supporting plate] for controlling operations of the display apparatus (Claims 1, 8, 15, 22, 29, 36) (JCC Ex. V, pp. 2-5)

This language does not need construction. If construed, CMO’s construction is preferable as LGD’s proposed construction inserts a negative requirement not mentioned in the claims that “no control circuit board is located on the back of the supporting plate or reflecting plate.”²² There is no basis for importing this limitation into the claims. Moreover, LGD asserts for certain limitations that the circuit board must be “mounted to” the side portion in question, insinuating that the circuit board must directly contact the side portion. Again, that is not a limitation of the invention described in the ‘926 patent.

LGD also asserts that independent claims 29 and 36 are indefinite. These claims contain the limitation “a circuit board installed on at least one of the side portions of [the reflecting plate/the supporting plate] for controlling operations of the display apparatus.” The references to “the reflecting plate” and “the supporting plate” in these claims should refer to “the integrated supporting unit.” This error is obvious on its face from the claims and the intrinsic record. CMO

²² LGD proposed construction is objectionable for the reasons stated above regarding “gap.”

asks that the Court correct this error. *Novo Indus., L.P. v. Micro Molds Corp.*, 350 F.3d 1348, 1354 (Fed. Cir. 2003) (court can correct a patent if: (1) "the correction is not subject to reasonable debate based on consideration of the claim language and the specification" and (2) "the prosecution history does not suggest a different interpretation of the claims.")

d. Integrated supporting unit (Claims 29, 36) (JCC Ex. V, p. 4)

The Court should construe this term as "a component including a supporting frame portion and either a reflecting plate portion or a supporting plate portion." The '926 specification makes clear that "[t]he only difference ... is that the [reflecting plate/supporting plate] ... incorporates the supporting frame ... to form an integrated supporting unit." 6:67-7:4, 7:27-32. LGD's proposed construction adds unnecessary ambiguity by using the term "unitary structure that provides support." In contrast, the language of the specification – which CMO used in its construction – is clear.

6. U.S. Patent No. 7,280,179 (JCC Ex. W)

The '179 patent teaches and claims an improved LCD device manufactured using the one drop fill method. Traditionally, LCD devices were manufactured by injecting liquid crystal through an injection hole left in the sealing material used to attach the two substrates together. 1:12-21. At the time of the '179 patent, the one drop fill (ODF) method of manufacture was replacing the traditional injection-based method. 1:21-38. The ODF method does not utilize an injection hole but, instead, requires "sealant [to be] applied to the *whole periphery* of one of a pair of substrates." 1:29-30 (emphasis added). Liquid crystal is then applied to one of the substrates which is then attached to the other substrate. 1:21-38. The '179 patent teaches implementation of the ODF method in a way that "more accurately control[s] the width of the sealing member," 2:59-61, while applying overlapping sealant to ensure complete enclosure of the display region. 4:20-23.

- a. **Forming a sealing member having a main portion enclosing a display region (Claim 1) (JCC Ex. W, p. 1)/The sealing member has a main portion enclosing a display region (Claims 5, 8) (JCC Ex. W, p. 2)**

These claim elements are clear on their face and should be given their plain and ordinary meaning. To the extent the Court believes the claim language requires construction, CMO proposes: “[forming] sealing material in a closed shape having four side walls for fixing a pair of substrates to each other and sealing the liquid crystal layer in the display region.” CMO’s construction is preferable to LGD’s because CMO’s construction clarifies the intrinsic record’s specific teaching that the sealant completely surround the display region in a closed shape. *See, e.g.*, 1:55-56 (“ensure that the formed sealing member can *fully enclose* the display region”) (emphasis added); 4/26/06 Office Action Response, Ex. W-2, at 8 (distinguishing this claim element from injection-based Choo patent, Ex. W-3) (“As can be seen with reference to FIG. 6 of Choo, the depicted seal line forms liquid crystal introducing inlet 37, and clearly *does not enclose* the display region of the depicted LCD module.”) (emphasis original).

- b. **Overlapping area extends along one side of the display region (Claims 1, 5, 8) (JCC Ex. W, p. 2)**

This claim element, including the claim term “overlapping,” is also clear on its face and should be given its plain and ordinary meaning. LGD’s construction imposes the overly restrictive limitation that “sealant material be applied on top of previously applied sealant material.” Indeed, applying one sealant directly on top of the other is not necessary “to ensure that the formed sealing member can fully enclose the display region,” which is the specification’s stated purpose for an overlapping area.²³ 1:53-56.

III. CONCLUSION

For all of the foregoing reasons, CMO respectfully requests that the Court enter an order adopting CMO’s proposed constructions for the disputed terms of the patents-in-suit.

²³ The parties also dispute the meaning of “applying the sealing material along the display region to form the main portion of the sealing member.” JCC Ex. W, p. 3. However, resolution of the disputed issues in the two claim elements discussed above will likewise resolve any dispute regarding this element. *Id.*

POTTER, ANDERSON & CORROON LLP

OF COUNSEL:

Jonathan S. Kagan
Alexander C.D. Giza
Adam Hoffman
Irell & Manella LLP
1800 Avenue of the Stars, Suite 900
Los Angeles, California 90067-4276
(310) 277-1010

Dated: August 11, 2008

By: /s/ Philip A. Rovner
Philip A. Rovner (#3215)
Hercules Plaza
1313 N. Market St.
P.O. Box 951
Wilmington, Delaware 19899-0951
(302) 984-6000
provner@potteranderson.com

*Attorneys for Defendant
Chi Mei Optoelectronics Corporation*

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

CERTIFICATE OF SERVICE

I, Philip A. Rovner, hereby certify that on August 11, 2008, the within document was filed with the Clerk of the Court using CM/ECF which will send notification of such filing(s) to the following; that the document was served on the following counsel as indicated; and that the document is available for viewing and downloading from CM/ECF.

BY CM/ECF, HAND DELIVERY AND E-MAIL

Richard E. Kirk, Esq.
Ashley Blake Stitzer, Esq.
The Bayard Firm
222 Delaware Avenue
Suite 900
P.O. Box 25130
Wilmington, DE 19899
rkirk@bayardfirm.com
astitzer@bayardfirm.com

BY CM/ECF, HAND DELIVERY AND E-MAIL

John W. Shaw, Esq.
Karen L. Pascale, Esq.
Young Conaway Stargatt & Taylor LLP
The Brandywine Building
1000 West Street, 17th Floor
Wilmington, DE 19801
jshaw@ycst.com
kpascale@ycst.com

I hereby certify that on August 11, 2008 I have sent by E-mail the foregoing document to the following non-registered participants:

Gaspare J. Bono, Esq.
Matthew T. Bailey, Esq.
Lora A. Brzezynski, Esq.
Cass W. Christenson, Esq.
R. Tyler Goodwyn, IV, Esq.
McKenna Long & Aldridge LLP
1900 K Street, NW
Washington, DC 20006
gbono@mckennalong.com
mbailey@mckennalong.com
lbrzezynski@mckennalong.com
cchristenson@mckennalong.com
tgoodwyn@mckennalong.com

Vincent K. Yip, Esq.
Peter J. Wied, Esq.
Jay C. Chiu, Esq.
Katherine F. Murray, Esq.
Ms. Denise Esparza
Paul Hastings Janofsky & Walker LLP
515 South Flower Street
Los Angeles, CA 90071
vincentyip@paulhastings.com
peterwied@paulhastings.com
jaychiu@paulhastings.com
katherinemurray@paulhastings.com
deniseesparza@paulhastings.com

Ron E. Shulman, Esq.
Julie M. Holloway, Esq.
Wilson Sonsini Goodrich & Rosati
650 Page Mill Road
Palo Alto, CA 94304-1050
rshulman@wsgr.com
jholloway@wsgr.com

M. Craig Tyler, Esq.
Brian D. Range, Esq.
Wilson Sonsini Goodrich & Rosati
8911 Capital of Texas Highway North
Westech 360, Suite 3350
Austin, TX 78759
ctyler@wsgr.com
brange@wsgr.com

/s/ Philip A. Rovner

Philip A. Rovner (#3215)
Potter Anderson & Corroon LLP
Hercules Plaza, 6th Floor
P. O. Box 951
Wilmington, DE 19899
(302) 984-6000
provner@potteranderson.com

846666

APPENDIX

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

LG DISPLAY CO., LTD.,

Plaintiff,

v.

CHI MEI OPTOELECTRONICS
CORPORATION, et al.,

Defendants.

Civil Action No. 06-726 (JJF)

Civil Action No. 07-357 (JJF)

CONSOLIDATED CASES

AMENDED JOINT CLAIM CONSTRUCTION CHARTS

Pursuant to the Court's May 19, 2008 Stipulation and Order Modifying the Scheduling Order (D.I. 208), LG Display Co., Ltd. and LG Display America, Inc. ("LG Display"), Chi Mei Optoelectronics Corporation and Chi Mei Optoelectronics USA, Inc. ("CMO"), and AU Optronics Corporation and AU Optronics Corporation America ("AUO") submit their Joint Claim Construction Charts as follows:

I. Patents asserted by LG Display:

U.S. Patent No. 4,624,737	Exhibit A
U.S. Patent No. 5,019,002	Exhibit B
U.S. Patent No. 5,825,449	Exhibit C
U.S. Patent No. 6,664,569	Exhibit D
U.S. Patent No. 6,803,984	Exhibit E
U.S. Patent No. 5,905,274	Exhibit F
U.S. Patent No. 6,815,321	Exhibit G
U.S. Patent No. 7,176,489	Exhibit H
U.S. Patent No. 7,218,374	Exhibit I

II. Patents asserted by AUO:

U.S. Patent No. 5,748,266	Exhibit J
U.S. Patent No. 6,689,629	Exhibit K
U.S. Patent No. 6,734,944	Exhibit L
U.S. Patent No. 6,778,160	Exhibit M
U.S. Patent No. 6,976,781	Exhibit N

U.S. Patent No. 7,090,506	Exhibit O
U.S. Patent No. 7,101,069	Exhibit P
U.S. Patent No. 7,125,157	Exhibit Q

III. Patents asserted by CMO:

U.S. Patent No. 5,619,352	Exhibit R
U.S. Patent No. 6,008,786	Exhibit S
U.S. Patent No. 6,013,923	Exhibit T
U.S. Patent No. 6,134,092	Exhibit U
U.S. Patent No. 6,734,926	Exhibit V
U.S. Patent No. 7,280,179	Exhibit W

Each party has listed what it contends is intrinsic evidence to support its contentions. All parties reserve the right to contest whether any such evidence is intrinsic or extrinsic.

August 6, 2008

/s/ Richard D. Kirk

OF COUNSEL:

Gaspere J. Bono
Song K. Jung
R. Tyler Goodwyn, IV
Lora A. Brzezynski
McKENNA LONG & ALDRIDGE LLP
1900 K Street, N.W.
Washington, D.C. 20006
(202) 496-7500

Richard D. Kirk (#0922)
Ashley B. Stitzer (#3891)
THE BAYARD FIRM
222 Delaware Avenue, 9th Floor
P.O. Box 25130
Wilmington, DE 19899-5130
(302) 655-5000
rkirk@bayardfirm.com
Attorneys for LG Display Co., Ltd. and LG Display America, Inc.

OF COUNSEL:

Jonathan S. Kagan
Alexander C.D. Giza
Adam Hoffman
IRELL & MANELLA LLP
1800 Avenue of the Stars, Suite 900
Los Angeles, California 90067-4276
(310) 277-1010

/s/ Philip A. Rovner

Philip A. Rovner (#3215)
POTTER ANDERSON & CORROON LLP
Hercules Plaza
P.O. Box 951
Wilmington, DE 19899
(302) 984-6000
provner@potteranderson.com
Attorneys for Chi Mei Optoelectronics Corporation and Chi Mei Optoelectronics USA, Inc.

OF COUNSEL:

/s/ Karen L. Pascale

Vincent K. Yip
Peter J. Wied
Terry Garnett
Katherine Murray
PAUL HASTINGS JANOFKY & WALKER LLP
515 South Flower Street, 25th Floor
Los Angeles, CA 90071
(213) 683-6000

M. Craig Tyler
Brian D. Range
WILSON SONSINI GOODRICH & ROSATI
8911 Capital of Texas Highway North
Westech 360, Suite 3350
Austin, TX 78759-8497
(512) 338-5400

Ron E. Shulman
Julie M. Holloway
WILSON SONSINI GOODRICH & ROSATI
650 Page Mill Road
Palo Alto, CA 94304-1050

John W. Shaw (#3362)
Karen L. Pascale (#2903)
YOUNG CONAWAY STARGATT & TAYLOR LLP
The Brandywine Building
1000 West Street, 17th Floor
P.O. Box 391
Wilmington, DE 19899-0391
(301) 571-6600
kpascale@ycst.com

*Attorneys for AU Optronics Corporation and AU
Optronics Corporation America*

EXHIBIT A

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT A
LG DISPLAY USP 4,624,737

Claim Terms	Des.	Agreed Constructions
insulating substrate	C	The material (such as glass, quartz, ceramic, insulator-coated silicon or insulator coated metal) upon which the transistor is fabricated to provide mechanical support and electrical insulation.

Disputed Constructions

Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
a process for producing a thin-film transistor	C	a method for manufacturing thin-film transistors such as for a liquid crystal display <u>Intrinsic Support</u> 1:6-29; 1:56-58; 1:61-68; 2:1-2; 2:8-68; 3:1-62; 4:1-23; Figs 1a-3d.	plain meaning in light of the construction below for “thin-film” transistor	Plain meaning.

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT A
LG DISPLAY USP 4,624,737

Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
thin-film transistor	C	<p>A three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.</p> <p><u>Intrinsic Support</u> 1:6-29; 1:56-58; 1:61-68; 2:1-2; 2:8-68; 3:1-62; 4:1-23; Figs 1a-3d.</p>	<p>A three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semi-conductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than in a single crystal silicon wafer.</p> <p><u>Intrinsic Support</u> 1:8-31; 1:47-53; 4:3-12 see also 5/5/05 Order re Claim Construction, Case No. 02-6775, at 13; Second Revised Joint Claim Construction Statement, Case No. 02-6775, at 89-93</p>	<p>Plain meaning.</p> <p>Alternate: A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.</p> <p><u>Intrinsic Support</u> E.g., Figs. 2-3; 1:8-29; 1:56-58; 2:8-4:2</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
forming a gate electrode on an insulating substrate	C	<p>giving form or shape to a patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode that is above and supported by or in contact with material (such as glass, quartz, ceramic, insulator-coated silicon or insulator coated metal) upon which the transistor is fabricated to provide mechanical support and electrical insulation</p> <p><u>Intrinsic Support</u></p> <p>1:14-21; 2:8-24; 3:21-39; Figs 1a-3d.</p>	plain meaning	<p>Producing a gate electrode above, supported by, and in contact with an insulating substrate</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2: 8-16; 3:23-28</p>
forming ... on	C	<p>giving form or shape to... above and supported by or in contact with</p> <p><u>Intrinsic Support</u></p> <p>1:14-17; 2:8-17; 3:21-39; Figs 1a, 2a, 3a.</p>	plain meaning	<p>Producing . . . above, supported by, and in contact with</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2: 8-16; 3:23-35</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film	C	<p>the formation of the gate insulating film, the high-resistivity semiconductor film and conducting film (without intervening films) above and supported by or in contact with (i) the patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode and (ii) the material (such as glass, quartz, ceramic, insulator-coated silicon or insulator coated metal) upon which the transistor is fabricated to provide mechanical support and electrical insulation.</p> <p><u>Intrinsic support</u></p> <p>1:14-53; 1:55-58; 2:8-45; 3:21-35; 3:54-62; 4:3-24; Figs 2a-3d; Abstract.</p>	<p>construe the term:</p> <p>"depositing on said gate electrode and substrate"</p> <p>as:</p> <p>depositing above and in contact with the gate electrode and the insulating substrate</p> <p><u>Intrinsic Support</u></p> <p>1:17-38; 3:28-35; 3:53-4:2; 4:17-23; Figs. 1a-1d, 2b, 3b (e.g., elements 1, 2, 3)</p>	<p>Precipitating a gate insulating film, a high resistivity semiconductor film and a conductive film on the gate electrode and the substrate without intervening films in between.</p> <p><u>Intrinsic Support</u></p> <p>E.g., Abstract; Figs. 2-3; 1:32-46; 2:17-53; 3:22-4:12</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
continuously depositing	L C A	<p>the formation of the gate insulating film, the high-resistivity semiconductor film and conducting film without intervening films</p> <p><u>Intrinsic Support</u></p> <p>1:17-21; 2:17-45; 3:28-35; 3:54-62; 4:1-13; Abstract; Figs 2b and 3b.</p>	<p>the formation of the gate insulating film, the high-resistivity semiconductor film and conducting film without intervening films</p> <p><u>Intrinsic Support</u></p> <p>1:17-38; 3:28-35; 3:53-4:2; 4:17-23; Figs. 1a-1d, 2b, 3b (e.g., elements 3, 4, 20 and 30) see also 5/5/05 Order re Claim Construction, Case No. 02-6775, at 8-9; Second Revised Joint Claim Construction Statement, Case No. 02-6775, at 95-101.</p>	<p>Precipitating... without intervening films</p> <p><u>Intrinsic Support</u></p> <p>E.g., Abstract; Figs. 2-3; 1:32-46; 2: 17-53; 3:22-4:12</p>
depositing on	C	<p>the formation of the gate insulating film, the high-resistivity semiconductor film and conducting film above and supported by or in contact with</p> <p><u>Intrinsic Support</u></p> <p>1:14-21; 2:8-45; 3:28-35; 3:54-62; 4:1-13; Abstract; Figs 2b and 3b.</p>	<p>this term should be construed as part of the larger term “depositing on said gate electrode and substrate”</p>	<p>precipitating above, supported by and in contact with</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:17-53; 3:22-4:12</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
depositing	A	<p>the formation of the gate insulating film, the high-resistivity semiconductor film and conducting film</p> <p><u>Intrinsic Support</u></p> <p>1:17-21; 2:17-45; 3:28-35; 3:54-62; 4:1-13; Abstract; Figs 2b and 3b.</p>	plain meaning	<p>Precipitating</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:17-53; 3:22 - 4:12</p>
gate insulating film	C	<p>a thickness of non-conductive material (such as SiNx) that has a high electrical resistance and insulates the transistor gate from the semiconductor.</p> <p><u>Intrinsic Support</u></p> <p>1:12-21, 2:18-38; 3:28-35; Abstract; Figs. 1b-1d, 2b-2e, and 3b-3d.</p>	<p>a thickness of material (such as SiNx, SiOx, or a multi-layer film made of such materials) with a high electrical resistance, spanning the region from the gate electrode to the high resistivity semiconductor layer, for insulating the gate electrode from the channel</p> <p><u>Intrinsic Support</u></p> <p>1:17-21; 4:17-23; 1:32-40; 4:47-53 (Claim 2); 4:26-46 (Claim 1); 3:53-4:2; Figs 2a-2e, 3</p>	<p>Plain meaning</p> <p>or</p> <p>Insulating film formed over the gate region</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:17-53; 3:22-4:12</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
high-resistivity semiconductor film	C	<p>a thickness of semiconductor material (such as amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline amorphous silicon) that has a higher resistance to current flow relative to the low-resistivity semiconductor film.</p> <p><u>Intrinsic Support</u></p> <p>1:8-29; 1:32-49; 2:17-32; 2:38-43; 2:54-60; 3:7-10; 3:16-21; 3:28-41; 4:48-62; 4:1-23; Abstract; Figs. 1b-1d, 2b-2e, and 3b-3d.</p>	<p>a thickness of semiconductor material (such as amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline amorphous silicon) that has a high resistance to current flow and acts as the channel of the transistor</p> <p><u>Intrinsic Support</u></p> <p>1:32-51; 2:8-10; 2:38-43; 2:60-3:4; Figs. 2b-2e, 3b-3d (e.g., element 4)</p>	<p>Plain meaning</p> <p>or</p> <p>Semiconductor having the property of high resistivity</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:17-53; 3:22-4:12</p>
conducting film	C	<p>a thickness of electrically conductive material</p> <p><u>Intrinsic Support</u></p> <p>1:25-29; 1:32-51; 2:10-36; 2:43-68; 3:1-10; 3:28-35; 3:48-62; 4:1-23; Abstract; Figs. 2b-2e and 3b-3d.</p>	<p>a thickness of electrically conductive material that lies adjacent to the channel layer</p> <p><u>Intrinsic Support</u></p> <p>2:17-21; 2:46-3:10; 3:53-4:2; Figs. 2b-2e, 3b-3d (e.g., elements 20, 30)</p>	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:17-53; 3:22-4:12</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
a conducting film containing at least a low-resistivity semiconductor film	L C A	<p>the conducting film is composed of a low-resistivity semiconductor film and possibly other conductive films</p> <p><u>Intrinsic Support</u></p> <p>1:18-36; 1:43-57; 2:17-37; 3:28-41; 3:48-62; 4:1-13, Abstract, Figs.2b-2e and 3b-3d.</p>	<p>plain meaning</p> <p>the terms "conducting film" and "low-resistivity semiconductor film" should be construed separately from this term</p>	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2: 17-53; 3:22-4:12</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
low-resistivity semiconductor film	C	<p>a thickness of semiconductor material (such as low-resistivity amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline amorphous silicon which contains phosphorous or other impurities to enhance the conductivity of the film) that has a lower resistance to current flow relative to the high-resistivity semiconductor film.</p> <p><u>Intrinsic Support</u></p> <p>1:25-29; 1:32-51; 2:17-50; 2:54-68; 3:1-10; 3:28-41; 3:48-62; 5:1-23; Abstract; Figs. 1d, 2b-2e, 3b-3d.</p>	<p>a thickness of semiconductor material (such as amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline amorphous silicon) that has a low resistance to current flow</p> <p><u>Intrinsic Support</u></p> <p>1:32-51; 2:17-21; 2:38-44; 3:53-4:2; Figs. 2b-2e, 3b-3d (e.g., element 20)</p>	<p>Plain meaning</p> <p>Or</p> <p>semiconductor having the property of low resistivity</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2: 17-53; 3:22 - 4:12</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
without exposing them to an oxidizing atmosphere	C	<p>without exposing the gate insulating film, the high-resistivity semiconductor film, and the conducting film containing at least the low-resistivity semiconductor film to an atmosphere that would create a detectable amount of oxidation on a film.</p> <p><u>Intrinsic Support</u></p> <p>1:32-46; 1:47-53; 2:17-36; 3:28-35; 3:53-62; 4:1-12; Figs. 2b-2e, 3b-3d.</p>	<p>without permitting the gate insulating film, high-resistivity semiconductor film, low-resistivity semiconductor film, or conducting film to come into contact with an uncontrolled ambient atmosphere which contains oxidizing agents</p> <p><u>Intrinsic Support</u></p> <p>1:32-51; 2:17-53; 3:28-35; Figs. 2b-2e, 3b-3d</p>	<p>Without exposing them to an atmosphere containing an oxidizing agent</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; Abstract; 1:32-46; 2:17-53; 3:22-4:12</p>
them	C	<p>the gate insulating film, the high-resistivity semiconductor film, and the conducting film containing at least the low-resistivity semiconductor film.</p> <p><u>Intrinsic Support</u></p> <p>2:17-36; 3:28-35; 3:53-62; 4:1-12; Abstract; Figs. 2b-2e, 3b-3d.</p>	<p>the gate insulating film, the high-resistivity semiconductor film, and the conducting film containing at least the low-resistivity semiconductor film</p>	<p>Indefinite.</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:17-53; 3:22-4:12</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
oxidizing atmosphere	C	<p>an atmosphere that would create a detectable amount of oxidation on a film.</p> <p><u>Intrinsic Support</u></p> <p>1:21-51; 2:17-53; 3:28-35; 3:53-4:23; Figs. 2b-2e, 3b-3d; Abstract.</p>	<p>an uncontrolled ambient atmosphere which contains oxidizing agents</p> <p><u>Intrinsic Support</u></p> <p>1:32-51; 2:17-53; 3:28-35; Figs. 2b-2e, 3b-3d</p>	<p>Atmosphere containing an oxidizing agent</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; Abstract; 1:32-46; 2:17-53; 3:22-4:12</p>
selectively etched	C	<p>The removal of selected portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) in order to produce a desired pattern on the surface.</p> <p><u>Intrinsic Support</u></p> <p>1:14-21; 1:25-29; 1:32-35; 2:10-16; 2:54-66; 3:7-10; 3:28-41; 3:44-48; 4:3-9; Figs 1a-d; 2a-e; 3a-d.</p>	<p>plain meaning</p>	<p>Selectively removed or corroded by a chemical agent</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:54-60; 3:22-4:12</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
they are partly left as an island region on said gate electrode	L	<p>a portion of the high resistivity semiconductor film and conducting film has been etched around its perimeter into a region located over the gate electrode of a thin-film transistor</p> <p><u>Intrinsic Support</u></p> <p>1:14-17; 1:25-29; 2:7-16; 2:54-66; 3:22-; Figs. 2-3.</p>	plain meaning	<p>Indefinite</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:54-60; 3:22-4:12</p>
island region on said gate electrode	C	<p>a portion of the high resistivity semiconductor film and conducting film has been etched around its perimeter into a region located over the gate electrode of a thin-film transistor.</p> <p><u>Intrinsic Support</u></p> <p>1:14-17; 1:25-29; 2:7-16; 2:54-66; 3:22-; Figs. 2-3.</p>	plain meaning	<p>Isolated region above, supported by, and in contact with the gate electrode</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:54-60; 3:22-4:12</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
gate electrode	C A	<p>a patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>1:14-18; 2:7-16; 3:33-29; Figs 1a-3d.</p>	<p>a patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>see 5/5/05 Order re Claim Construction, Case No. 02-6775, at 7-8; Second Revised Joint Claim Construction Statement, Case No. 02-6775 at 93-95</p>	<p>A patterned, electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:8-16; 3:23-28</p>
a fourth step for selectively forming a source electrode and drain electrode	C A	<p>forming a source electrode and drain electrode in selected regions only</p> <p><u>Intrinsic Support</u></p> <p>1:21-29; 1:32-51; 2:17-68; 3:1-14; 3:28-62; 4:1-12; Abstract; Figs. 1d, 2d-2e, 3c-3d.</p>	plain meaning	<p>Step-plus function element.</p> <p>Function is "selectively forming a source electrode and drain electrode"</p> <p>Step is disclosed: E.g., Figs. 2-3; 2:60-3:10; 3 :22-4:12</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
selectively forming	C	forming in selected regions only <u>Intrinsic Support</u> 1:14-17; 1:25-29; 2:10-36; 2:60-68; 3:1-10; 3:24-52; 4:3-9; Abstract; Figs. 1a-1d, 2a-2e, 3a-3d.	plain meaning	Selectively producing <u>Intrinsic support</u> E.g., Figs. 2-3; 2:60-3:10; 3 :22-4:12

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
source electrode	C A	<p>a patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.</p> <p><u>Intrinsic Support</u></p> <p>1:21-29; 1:32-51; 2:17-68; 3:1-14; 1:28-62; 4:1-12; Abstract; Figs 1d, 2d-2e, 3c-3d.</p>	<p>construe term:</p> <p>"a source electrode and a drain electrode"</p> <p>as:</p> <p>Patterned, electrically conductive material formed over the source region and drain region, respectively, of a transistor. Current flows through the channel between the source electrode and the drain electrode of the transistor under control of the gate electrode of the transistor.</p> <p><u>Intrinsic Support</u></p> <p>1:32-51; 2:60-66; 3:4-7; 3:36-41; 3: 59-4:6; Figs. 2d 2e, 3c-3d (e.g., elements 5, 6)</p>	<p>A patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.</p> <p><u>Intrinsic Support</u></p> <p>E.g., Abstract; 1:17-29; 2:60-3:10; 3:36-41</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
drain electrode	C A	<p>a patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source and drain electrode under the control of the gate electrode.</p> <p><u>Intrinsic Support</u></p> <p>1:21-29; 1:32-51; 2:17-68; 3:1-14; 3:28-62; 4:1-12; Abstract; Figs. 1d, 2d-2e, 3c-3d.</p>	<p>this term should be construed as part of the larger term “a source electrode and a drain electrode”</p>	<p>A patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.</p> <p><u>Intrinsic Support</u></p> <p>E.g., Abstract; 1:17-29; 2:60-3:10; 3:36-41</p>
contacting a part of the surface of said island region	L C A	<p>touching a part of the surface of the island region</p> <p><u>Intrinsic Support</u></p> <p>2:54-3:10; 3:53-62; 4:1-2; Figs 2d-2e; 3c-3d.</p>	<p>Touching a part of the surface of the island region</p> <p><u>Intrinsic Support</u></p> <p>2:60-66; 3:4-7; 3:36-41 Figs. 2d-2e, 3c-3d</p>	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:60-3:10; 3:22-4:12</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask	A	<p>a fifth step for removing selected regions only of the conducting film on the island region not covered by the source electrode, drain electrode or mask wherein the source electrode and drain electrode serve as at least a part of the pattern above a surface from which material is to be selectively removed; the pattern is made of material that is resistive to the removal technique relative to the material to be removed</p> <p><u>Intrinsic Support</u></p> <p>1:14-54; 2:10-14; 2:54-68; 3:1-16; 3:24-52; Abstract; Figs 1a-1d, 2a-2e, 3a-3d.</p>	<p>eliminating all the conducting film in the space between the edges of the source and drain electrodes</p> <p><u>Intrinsic Support</u></p> <p>1:32-51; 2:60-66; 3:8-10; 3:36-41; 3:59-4:6; Figs. 2c-2e, 3b-3d</p>	<p>a fifth step for using the source and drain electrodes to partially define the boundary for the removal of the conducting film exposed on the island region.</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:60-3:10; 3:22-4:12</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
selectively removing said conducting film exposed on said island region	C	removing selected regions only of the conducting film on the island region not covered by the source electrode, drain electrode or mask <u>Intrinsic Support</u> 1:14-54; 2:10-14; 2:54-68; 3:1-16; 3:24-52; Abstract; Figs 1a-1d, 2a-2e, 3a-3d.	eliminating all the conducting film in the space between the edges of the source and drain electrodes <u>Intrinsic Support</u> 1:8-31; 1:32-51; 2:60-66; 3:8-10; 3:36-41; 3:59-4:6; Figs. 1b-1d, 2c-2e, 3b-3d	Plain meaning <u>Intrinsic Support</u> E.g., Figs. 2-3; 2:60-3:10; 3:22-4:12
selectively removing	C	removing selected regions only <u>Intrinsic Support</u> 1:14-29; 2:10-14; 2:54-68; 3:1-16; 3:24-52; Abstract; Figs 1a-1d, 2a-2e, 3a-3d.	this term should be construed as part of the larger term, “selectively removing said conducting film exposed on said island region.”	Plain meaning <u>Intrinsic Support</u> E.g., Figs. 2-3; 2:60-3:10; 3:22-4:12
said conducting film exposed on said island region	A	the conducting film on the island region that is not covered by the source electrode, drain electrode or mask <u>Intrinsic Support</u> 1:14-54; 2:10-14; 2:54-68; 3:1-16; 3:24-52; Abstract; Figs 1a-1d, 2a-2e, 3a-3d.	Plain meaning	the conducting film on top of the island region exposed to the atmosphere <u>Intrinsic Support</u> E.g., Figs. 2-3; 2:60-3:10; 3:22-4:12

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
said source and drain electrodes serving as at least a part of the mask	C A	the source and drain electrodes serving as at least a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of material that is resistive to the removal technique relative to the material to be removed <u>Intrinsic Support</u> 1:14-54; 2:10-14; 2:54-68; 3:1-16; 3:24-52; Abstract; Figs. 1a-1d, 2a-2e, 3a-3d.	the source and drain electrodes are part of the pattern on the top surface that protects underlying layer from being removed while allowing the portion of the layer exposed between the source and drain electrodes to be removed <u>Intrinsic Support</u> 1:8-31; 1:32-51; 2:60-66; 3:8-10; 3:36-41; 3:59-4:6; Figs. 1b-1d, 2c-2e, 3b-3d	Using the source and drain electrodes to partially define the boundary for the removal or formation of the conductive film. <u>Intrinsic Support</u> E.g., Figs. 2-3; 2:60-3:10; 3:22-4:12
serving as at least a part of the mask	L	serving as at least a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of material that is resistive to the removal technique relative to the material to be removed <u>Intrinsic Support</u> 1:14-29; 2:10-14; 2:54-68; 3:1-16; 3:24-52; Abstract; Figs. 1a-1d, 2a-2e, 3a-3d.	this term should be construed as part of the term "said source and drain electrodes serving as at least a part of the mask" see also construction of "mask" below <u>Intrinsic Support</u> 1:8-31; 1:32-51; 2:60-66; 3:8-10; 3:36-41; 3:59-4:6; Figs. 1b-1d, 2c-2e, 3b-3d	using ... to partially define the boundary for the removal process <u>Intrinsic Support</u> E.g., Figs. 2-3; 2:60-3:10; 3:22-4:12

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
at least a part of the mask	C	<p>at least a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of material that is resistive to the removal technique relative to the material to be removed.</p> <p><u>Intrinsic Support</u></p> <p>1:14-29; 2:10-14; 2:54-68; 3:1-16; 3:24-52; Abstract; Figs 1a-1d, 2a-2e, 3a-3d.</p>	this term should be construed as part of the term “said source and drain electrodes serving as at least a part of the mask”	<p>to partially define the boundary for the removal or formation process</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3, 2:60-3:10; 3:22-4:12</p>
a part of the mask	A	<p>a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of material that is resistive to the removal technique relative to the material to be removed.</p> <p><u>Intrinsic Support</u></p> <p>1:14-29; 2:10-14; 2:54-68; 3:1-16; 3:24-52; Abstract; Figs 1a-1d, 2a-2e, 3a-3d.</p>	this term should be construed as part of the term “said source and drain electrodes serving as at least a part of the mask”	<p>to partially define the boundary for the removal or formation process</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:60-3:10; 3:22-4:12</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
mask	A	<p>A pattern above a surface from which material is to be selectively removed. The pattern is made of material that is resistive to the removal technique relative to the material to be removed.</p> <p><u>Intrinsic Support</u></p> <p>1:14-29; 2:10-14; 2:54-68; 3:1-16; 3:24-52; Abstract; Figs 1a-1d, 2a-2e, 3a-3d.</p>	<p>A top surface pattern above one or more layers of material that will be selectively removed according to the shape of the mask. The mask is made of material that is resistive to the removal technique and defines by its edges the boundaries of the material selected for removal.</p> <p><u>Intrinsic Support</u></p> <p>1:8-31; 1:32-51; 2:60-66; 3:8-10; 3:36-41; 3:59-4:6; Figs. 1b-1d, 2c-2e, 3b-3d</p>	<p>A pattern to define the boundary for the removal or formation process</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:60-3:10; 3:22-4:12</p>
surface passivation film	C	<p>a thickness of material that provides protection such as electrical stability and chemical isolation</p> <p><u>Intrinsic Support</u></p> <p>1:29-31; 3:11-21; 3:44-48; Figs 2e, 3d.</p>	<p>plain meaning</p>	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 3:11-21; 3:22-4:12</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
exposing a part of each of said source electrode, drain electrode and gate electrode	C A	removing portions of one or more layers to uncover a part of each of said source electrode, drain electrode and gate electrode <u>Intrinsic Support</u> 1:6-31; 3:11-21; 3:36-52; Fig. 2e; 3d.	plain meaning	causing a part of the source electrode, drain electrode and gate electrode to be exposed to the atmosphere <u>Intrinsic Support</u> E.g., Figs. 2-3; 3:11-21; 3:22-4:12
exposing	A	removing portions of one or more layers to uncover <u>Intrinsic Support</u> 1:6-31; 3:11-21; 3:36-52; Fig. 2e; 3d.		Uncovering <u>Intrinsic Support</u> E.g., Figs. 2-3; 3:11-21; 3:22-4:12

EXHIBIT B

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT B
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Disputed Constructions

Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
substrate	C	<p>the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support</p> <p><u>Intrinsic Support:</u></p> <p>1:34-38; 3:33-38; Figs. 1-7; Abstract.</p>	<p>Plain meaning</p>	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 1-2; 37-38; 4:11-22; 4:67-5:2</p>
forming a pattern of pixels on said substrate	C	<p>depositing and etching a matrix of transparent electrically conductive material to form pixel electrodes above and supported by or in contact with the substrate</p> <p><u>Intrinsic Support</u></p> <p>1:38-2:6; 2:45-68; 3:3-21; 3:25-36; 3:47-59; 4:4-22, 4:42-45; 4:61-5:6, 5:24-32; 5:42-5:57; 6:46-6:50; 6:60-7:18; 7:47-7:60; 8:49-62; Figs. 1, 4-7; Figs. 1-6; Abstract.</p>	<p>forming a repeating configuration of redundant subpixels</p> <p><u>Intrinsic Support</u></p> <p>7:46-60; 4:58-60; 5:44-57; 6:19-25; 6:26-36; and figures referenced therein</p>	<p>Forming a pattern of pixels above, supported by and in contact with the substrate</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 1, 2, 3, & 6; 3:25-4:3; 5:2-6; 5:24-32</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
forming a plurality of row and column intersecting pixel activation lines	C	depositing and etching electrically conductive material patterned in rows and columns that control pixels <u>Intrinsic Support</u> 1:38-42; 1:56-59-2:6; 2:54-62; 3:33-54, 3:60-63; 4:45-58; 5:58-6:17; 6:25-59; 7:3-15; 7:23-29; Figs. 1, 4-7; Abstract.	forming a plurality of row intersecting pixel activation lines and column intersecting pixel activation lines <u>Intrinsic Support</u> 6:1-18; 6:26-36; 5:58-68; 6:38-50; 7:3-10; and figures referenced therein	forming a plurality of row intersecting pixel activation lines and a plurality of column intersecting pixel activation lines <u>Intrinsic Support</u> E.g., Figs. 1, 4, 5, & 6; 3:25-4:3; 5:44-7:10

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another	A	electrically connecting with conductive material all or nearly all row lines to at least one other row line and electrically connecting with conductive material all or nearly all of the column lines to at least one other column line <u>Intrinsic Support</u> 1:34-35; 5:65-68; 6:6-17; 6:26-32; 6:38-60; 8:1-37; 8:49-62, Fig. 4-7.	electrically connecting with conductors nearly all, but not all, of said row lines to one another and nearly all, but not all, of said column lines to one another <u>Intrinsic Support</u> 5:65-68; 6:6-9; 6:42-43; 8:5-7; and figures referenced therein see also June 13, 2006 Memorandum Opinion 4-6	joining almost all of the row lines together and joining almost all of the column lines together <u>Intrinsic Support</u> E.g., Figs. 1, 4, 5, 6 & 7; 3:25-4:3; 5:44-7:10; 8:1-48; U.S. Pat. No. 4,820,222: Figs. 1, 6, 7, & 8; 7: 39-8:34 App 07/218312, 3/31/89 OA, Pages 2-3; App 07/218312, 6/25/90 Proposed Response, Pages 2-3 App 06/948224, 3/16/88 Office Action, Pages 3-4; App 06/948224, 9/16/88 Response, Pages 7-9

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
interconnecting	L C	electrically connecting with conductive material <u>Intrinsic Support</u> 1:34-35; 5:65-68; 6:6-17; 6:26-32; 6:38-60; 8:1-37; 8:49-62, Fig. 4-7; App 07/218,312, 3/31/1989, Office Action, pages 2-4; App 07/218,312, 7/12/1990, Response, pages 2-3.	electrically connecting with conductors <u>Intrinsic Support</u> 5:65-68; 6:6-9; 6:42-43; 8:5-7; and figures referenced therein see also June 13, 2006 Memorandum Opinion 4-6	Joining together <u>Intrinsic Support</u> E.g., Figs. 1, 4, 5, 6 & 7; 3:25-4:3; 5:44-7:10; 8:1-48 U.S. Pat. No. 4,820,222: Figs. 1, 6, 7, & 8; 7: 39-8:34 App 07/218312, 3/31/89 OA, Pages 2-3 App 07/218312, 6/25/90 Proposed Response, Pages 2-3 App 06/948224, 3/16/88 Office Action, Pages 3-4; App 06/948224, 9/16/88 Response, Pages 7-9
substantially all	C A	all or nearly all <u>Intrinsic Support</u> 1:34-35; 5:65-68; 6:6-17; 6:26-32; 6:38-60; 8:1-37; 8:49-62; Fig. 4-7.	nearly all, but not all <u>Intrinsic Support</u> 1:15-35; 1:56-2:10; 2:45-51; 4:9-31; and figures referenced therein	Almost all <u>Intrinsic Support</u> E.g., Figs. 1, 4, 5, 6 & 7; 3:25-4:3; 5:44-7:10; 8:1-48 U.S. Pat. No. 4,820,222: Figs. 1, 6, 7, & 8; 7:39-8:34

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
row lines	C	<p>electrically conductive material patterned in rows that control pixels</p> <p><u>Intrinsic Support</u></p> <p>1:38-42; 1:56-59-2:6; 2:54-62; 3:33-54, 3:60-63; 4:45-58; 5:58-6:17; 6:25-59; 7:3-15; 7:23-29; Figs. 1, 4-7; Abstract.</p>	<p>Indefinite</p> <p>or</p> <p>lines connecting all pixels in a row</p> <p><u>Intrinsic Support</u></p> <p>1:38-42; 3:37-46; and figures referenced therein</p>	<p>Indefinite; or Lines connecting all pixels in a row</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 1, 4, 5, 6 & 7; 3:25-4:3; 5:44-7:10; 8:1-48 U.S. Pat. No. 4,820,222: Figs. 1, 6, 7, & 8; 7: 39-8:34</p>
column lines	C	<p>electrically conductive material patterned in columns that control pixels</p> <p><u>Intrinsic Support</u></p> <p>1:38-42; 1:56-59-2:6; 2:54-62; 3:33-54, 3:60-63; 4:45-58; 5:58-6:17; 6:25-59; 7:3-15; 7:23-29; Figs. 1, 4-7; Abstract.</p>	<p>indefinite</p> <p>or</p> <p>lines connecting all pixels in a column</p> <p><u>Intrinsic Support</u></p> <p>1:38-42; 3:37-46; and figures referenced therein</p>	<p>Indefinite; or Lines connecting all pixels in a column</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 1, 4, 5, 6 & 7; 3:25-4:3; 5:44-7:10; 8:1-48 U.S. Pat. No. 4,820,222: Figs. 1, 6, 7, & 8; 7:39-8:34</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
row and column lines	C	<p>electrically conductive material patterned in rows and columns that control pixels</p> <p><u>Intrinsic Support</u></p> <p>1:38-42; 1:56-59-2:6; 2:54-62; 3:33-54, 3:60-63; 4:45-58; 5:58-6:17; 6:25-59; 7:3-15; 7:23-29; Figs. 1, 4-7; Abstract.</p>	<p>Indefinite</p> <p>or</p> <p>the row lines and the column lines</p> <p><u>Intrinsic Support</u></p> <p>1:38-42; 3:37-46; and figures referenced therein</p>	<p>Indefinite; or The row lines and the column lines</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 1, 4, 5, 6 & 7; 3:25-4:3; 5:44-7:10; 8:1-48 U.S. Pat. No. 4,820,222: Figs. 1, 6, 7, & 8; 7:39-8:34</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
outer electrostatic discharge guard ring	L C A	<p>a closed or open ring, or open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharge</p> <p><u>Intrinsic Support</u></p> <p>1:8-14; 2:37-68; 3:20-21; 4:22-31; 4:46-60; 7:11-22; 7:30-34; 8:1-17; 8:24-37; 8:40-44; 8:49-62; Abstract; Figs. 5-7; App 07/218,312, 3/31/1989, Office Action, pages 2-4; App 07/218,312, 7/12/1990, Proposed Response, page 2-3.</p>	<p>a closed or open ring, or open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharges</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:61-62; 8:27-29; and figures referenced therein see also June 13, 2006 Memorandum Opinion 7-10</p>	<p>A surrounding structure outside the active matrix display to provide protection from electrostatic discharges</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 4, 5, 6 & 7; 3:25-4:3; 5:44-7:10; 8:1-48</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
resistance	L C A	<p>a circuit component designed to provide opposition to electric current flowing through itself and to minimize current surge in the TFT array from electrostatic discharge</p> <p><u>Intrinsic Support</u></p> <p>1:8-14; 2:45-68; 4:46-60; 5:32-43; 7:14-18; 7:35-46; 7:61-68; 8:18-39; 8:49-62; Abstract; App 07/218,312, 3/31/1989, Office Action, pages 2-4; App 07/218,312, 7/12/1990, Response, pages 2-3.</p>	<p>a circuit component that has a specified resistance to the flow of electric current and is used to minimize the current surge from an electrostatic discharge</p> <p><u>Intrinsic Support</u></p> <p>8:23-34; and figures referenced therein see also June 13, 2006 Memorandum Opinion 10-13</p>	<p>A circuit component that has a specified ratio between voltage and the flow of electric current, and used to minimize the current surge from electrostatic discharge.</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 4, 5, 6 & 7; 3:25-4:3; 5:44-7:10; 8:1-48</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays	A	<p>to minimize current surge in the TFT array from electrostatic discharge during manufacture of the display</p> <p><u>Intrinsic Support</u></p> <p>1:8-14; 2:45-68; 4:46-60; 5:32-43; 7:14-18; 7:35-46; 7:61-68; 8:23-39; 8:49-62; Abstract; Fig. 5, 7.</p>	Indefinite	<p>To guard against electrostatic discharges between the row activation lines and column activation lines during the manufacturing of the displays</p> <p><u>Intrinsic Support'</u></p> <p>E.g., 4:9-6:59; 9:1-48</p>
protection from electrostatic discharges	C	<p>to minimize current surge in the TFT array from electrostatic discharge during manufacture of the display</p> <p><u>Intrinsic Support</u></p> <p>1:8-14; 2:45-68; 4:46-60; 5:32-43; 7:14-18; 7:35-46; 7:61-68; 8:23-39; 8:49-62; Abstract; Fig. 5, 7.</p>	Indefinite	<p>Plain meaning;</p> <p>or</p> <p>Guarding against electrostatic discharges</p> <p><u>Intrinsic Support</u></p> <p>E.g., 4:9-6:59; 8:1-48</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
row and column activation lines	C	<p>electrically conductive material patterned in rows and columns that control pixels</p> <p><u>Intrinsic Support</u></p> <p>1:38-42; 1:56-59-2:6; 2:54-62; 3:33-54, 3:60-63; 4:45-58; 5:58-6:17; 6:25-59; 7:3-15; 7:23-29; Figs. 1, 4-7; Abstract.</p>	<p>indefinite</p> <p>or</p> <p>control lines activating all pixels in rows and control lines activating all pixels in columns</p> <p><u>Intrinsic Support</u></p> <p>1:38-42; 2:4-7; 3:37-46; and figures referenced therein</p>	<p>Indefinite;</p> <p>or</p> <p>Control lines activating all pixels in rows and control lines activating all pixels in columns.</p> <p><u>Intrinsic Support</u></p> <p>E.g., 4:9-6:59; 8 : 1-48</p>
removing said outer guard ring and row and column interconnections	L C	<p>physically disconnecting said guard ring and row and column interconnections</p> <p><u>Intrinsic Support</u></p> <p>2:45-68; 8:11-17; 8:26-30; 8:40-62; Abstract; App 07/218,312, 3/31/1989, Office Action, pages 2-4; App 07/218,312, 7/12/1990, Response, pages 2-3.</p>	<p>physically disconnecting said guard ring and row and column interconnections</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:64-65; 8:27-30; and figures referenced therein</p>	<p>Indefinite; physically disconnecting said guard ring and lines connecting the row and column , intersecting pixel activation lines from the substrate</p> <p><u>Intrinsic Support</u></p> <p>E.g., Fig. 7; 2:45-68; 8:1-48 App 07/218312, 3/31/89 OA, Pages 2-3 App 07/218312, 6/25/90 Proposed Response, Pages 2-3 U.S. Pat. No. 4,820,222: Figs. 6 & 8; 6: 42-7:38</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
removing	A	<p>physically disconnecting said guard ring and row and column interconnections</p> <p><u>Intrinsic Support</u></p> <p>2:45-68; 8:11-17; 8:26-30; 8:40-62; Abstract; App 07/218,312, 3/31/1989, Office Action, pages 2-4; App 07/218,312, 7/12/1990, Response, pages 2-3.</p>	<p>physically disconnecting</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:64-65; 8:27-30; and figures referenced therein</p>	<p>Taking away</p> <p>Alternate 1: separating or breaking off</p> <p>Alternate 2: physically disconnecting</p> <p><u>Intrinsic Support</u></p> <p>E.g., Fig. 7; 2:45-68; 8:1-48 App 07/218312, 2/31/89 OA, Pages 2-3 App 07/218312, 7/22/90 Proposed Response, Pages 2-3 U.S. Pat. No. 4,820,222: Figs. 6 & 8; 6: 42-7:38</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT B
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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
inner electrostatic discharge guard ring	L C	a closed or open ring, or open L or C-shaped line, inside the source and/or gate pads to provide protection from electrostatic discharge <u>Intrinsic Support</u> 1:8-14; 2:45-68; 4:46-60; 5:32-43; 6:60-72; 7:14-68; 8:49-62, Abstract.	a closed or open ring, or open L or C-shaped conductive line, inside the active matrix display to provide protection from electrostatic discharges <u>Intrinsic Support</u> 7:14-21; 7:22-68; and figures referenced therein see also June 13, 2006 Memorandum Opinion 7-10; LGD's Mar. 8, 2006 Plaintiffs Memorandum in Support of Its Proposed Claim Constructions 15-17	Ring structure inside the active matrix display to provide protection from electrostatic discharges <u>Intrinsic Support</u> E.g., Fig. 5; 2:45-68; 6:60-7:68

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT B
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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
shunt switching elements	C A	shunt transistors, including floating gate, no gate, an oxide below to form a spark gap, or other active switching elements such as diodes <u>Intrinsic Support</u> 7:22-50; 7:61-68; 8:49-62; Abstract.	an active switching element like a shunt transistor or diode <u>Intrinsic Support</u> 8:57-59; 8:18-27; 8:34-39; and figures referenced therein see also LGD's Mar. 8, 2006 Plaintiff's Memorandum in Support of Its Proposed Claim Constructions 19-20.	A switching circuit for shunting electrostatic discharges <u>Intrinsic Support</u> E.g., Fig. 5; 2:45-68; 6:60-7:68

EXHIBIT C

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT C
LG DISPLAY USP 5,825,449

Claim Terms	Des.	Agreed Constructions
substrate	C	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.
indium tin oxide layer	C	a thickness of indium tin oxide (ITO)
contact hole is provided through ... layer(s)	C A	the contact hole is formed in the layer(s)

Disputed Constructions

Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
wiring structure	C	<p>a structure electrically connecting at least two points</p> <p><u>Intrinsic Support</u></p> <p>4:24-27; Figs. 1-3.</p>	<p>a structure providing an electrically conductive path that connects at least two terminals</p> <p><u>Intrinsic Support</u></p> <p>1:52-54; 2:16-18; 4:1-5; 4:24-26; Figs. 4, 6; 5/5/05 Order re Claim Construction, Case No. 02 6775, at 13; Second Revised Joint Claim Construction Statement, Case No. 02 6775, at 179</p>	<p>A structure made by wires</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-5; 2:31-3:14</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT C
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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
conductive layer	L C	thickness of electrically conductive material <u>Intrinsic Support</u> 1:34-38; 2:31-3:15; 3:44-50; 4:50-53; 4:65-5:22; Fig 1-3.	a thickness of electrically conductive material that may include one or more patterned features, all of a single material <u>Intrinsic Support</u> 1:34-37; 1:56-60; 1:61-64; 2:37-46; 3:44-47; 4:50-53; 4:61-5:22; 7:36-39 (claim 10); Figs. 1a, 1e, 2a, 2e, 3; '449 File history, 8/1/97 Office Action, para. 2.	Plain meaning
layer	C	a thickness of material <u>Intrinsic Support</u> 1:34-38; 2:31-3:15; 3:44-50; 4:50-53; 4:65-5:22; Fig 1-3.	plain meaning	Plain meaning
formed on a first portion of said substrate	C	above and in contact with a first part of the substrate <u>Intrinsic Support</u> 1:31-48; 1:56-64; 2:37-46; 3:44-62; 4:19-23; 4:39-41; 4:65-5:8; Figs 2-3; App. No. 08/781,188, 8/1/97, Office Action, page 2.	above and in contact with a first part of the substrate <u>Intrinsic Support</u> 1:56-60; Figs. 1a, 1e, 2a, 2e, 3	Produced above, supported by, and in contact with a first portion of the substrate <u>Intrinsic Support</u> E.g., Figs. 3, 4, & 5; 4:46-4:64; 4:65-5:5; 5:23-38; 5:39-54

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT C
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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
formed on	C A	<p>above and in contact with</p> <p><u>Intrinsic Support</u></p> <p>1:31-48, 56-64; 2:37-46; 3:44-62; 4:19-23; 4:39-41; 4:65-5:8; Figs 2-3; App. No. 08/781,188, 8/1/97, Office Action, page 2.</p>	<p>above and in contact with</p> <p><u>Intrinsic Support</u></p> <p>1:35-38, 1:42-44, 1:44-48, 2:37-40, 2:42-44, 3:44-47, 3:56-60; Figs. 1a-lf, 2a-2e, 3</p>	<p>Produced above, supported by, and in contact with</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 4:46-4:64; 4:65-5:5; 5:23-38; 5:39-54</p>
formed on a second portion of said substrate	C	<p>above and in contact with a second part of the substrate</p> <p><u>Intrinsic Support</u></p> <p>1:31-48, 56-64; 2:37-46; 3:44-62; 4:19-23; 4:39-41; 4:65-5:8; Figs 2-3; App. No. 08/781,188, 8/1/97, Office Action, page 2.</p>	<p>above and in contact with a second part of the substrate</p> <p><u>Intrinsic Support</u></p> <p>1:35-38, 3:44-47; Figs. 2b, 3</p>	<p>Produced above, supported by, and in contact with a second portion of the substrate</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 4:46-4:64; 4:65-5:5; 5:23-38; 5:39-54</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
formed on a first portion of said first insulative layer	C	<p>above and in contact with a first part of the first insulative layer</p> <p><u>Intrinsic Support</u></p> <p>1:31-48, 56-64; 2:37-46; 3:44-62; 4:19-23; 4:39-41; 4:65-5:8; Figs 2-3; App. No. 08/781,188, 8/1/97, Office Action, page 2.</p>	<p>above and in contact with a first part of the first insulative layer</p> <p><u>Intrinsic Support</u></p> <p>1:42-44; Figs. 2b, 3, 5</p>	<p>Produced above, supported by, and in contact with a first portion of the first insulative layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 4:46-4:64; 5:6-5:15; 5:23-38; 5:39-54</p>
insulative layer	C	<p>a thickness of non-conductive material (such as SiNx) that has high electrical resistance</p> <p><u>Intrinsic Support</u></p> <p>1:40-42; 2:5-9, 2:40-41, 45-51, 61-62; 3:1-8, 50-54; 4:6-12, 27-34, 47-50; 5:1-2, 8-15; Figs. 1-3.</p>	Plain meaning	Plain meaning

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer	C	<p>above and in contact with the second conductive layer and above and in contact with a second part of the first insulative layer above the first conductive layer</p> <p><u>Intrinsic Support</u></p> <p>1:31-48, 56-64; 2:37-46: 3:44-62; 4:19-23; 4:39-41; 4:65-5:8; Figs 2-3; App. No. 08/781,188, 8/1/97, Office Action, page 2.</p>	<p>above and in contact with the second conductive layer and above and in contact with a second part of the first insulative layer above the first conductive layer</p> <p><u>Intrinsic Support</u></p> <p>Figs. 1f, 2d, 3 (e.g., element 9)</p>	<p>Produced above, supported by, and in contact with the second conductive layer and a second portion of the insulative layer covering the top surface of the first conductive layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 4:46-4:64; 5:6-5:15; 5:23-38; 5:39-54</p>
overlying	C	<p>above</p> <p><u>Intrinsic Support</u></p> <p>1:40-44; 2:37-55; 3:63-4:15; 5:16-22; Figs 1-3.</p>	<p>this term should be construed as part of the larger term ("formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer")</p> <p><u>Intrinsic Support</u></p> <p>1:40-44; Fig. 1b</p>	<p>Covering the top surface of</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 4:46-4:64; 5:6-5:15; 5:23-38; 5:39-54</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
contact hole	C	<p>an opening in one or more insulative layers to expose a portion of a conductive layer for purposes of forming an electrical connection.</p> <p><u>Intrinsic Support</u></p> <p>1:51-2:10; 2:31-3:14; 3:50-4:41; 4:47-5:47; Figs. 1-3.</p>	<p>an opening formed in one or more insulative layers to expose a portion of a conductive layer for purposes of forming an electrical connection</p> <p><u>Intrinsic Support</u></p> <p>2:46-55, 3:2-14, 4: 8-15, 4: 53-64, 5:8-13, 5:19-22, 5:33-36; Figs. 2d-2e, 3 and 5</p>	Plain meaning
provided through	C	<p>the contact hole is formed in the layer</p> <p><u>Intrinsic Support</u></p> <p>1:51-2:10; 2:31-3:14; 3:50-4:41; 4:47-5:47; Figs. 1-3.</p>	plain meaning	See above
expose part of said ... layer	C	<p>removing portions of one or more layers to uncover at least part of another layer</p> <p><u>Intrinsic Support</u></p> <p>1:52-60; 2:5-10, 17-28, 45-55; 3:1-14, 3:66-4:15; 4:35-39, 46-50; 5:8-22; Figs. 1-3; Abstract.</p>	plain meaning	Plain meaning

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
extends through	C	is disposed in <u>Intrinsic Support</u> 1:50-60; 2:36-3:15; 4:16-34; 4:47-64; 5:5-23; Figs 1-3.	plain meaning	Plain meaning
one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor	C A	one, but not both, of the first and second conductive layers is directly connected to one terminal of a thin film transistor <u>Intrinsic Support</u> 1:24-30; 2:31-3:15; 3:63-4:5; 4:46-5:23; Fig 3; App. No. 08/781,188, 12/1/1997, Amendment, at p. 5-7.	the first conductive layer is connected to the gate, source or drain of a thin film transistor, and/or the second conductive layer is connected to the gate, source or drain of the thin film transistor <u>Intrinsic Support</u> 2:16-28, 4:1-5; 4:65-5:13; 5:16-22; 5:23-39; 5:40-51, Figs. 3, 4, 5; `449 File history, 8/1/97 Office Action, para. 6; `449 File history, 12/1/1997 Amendment & Response, pages 1-7; Claims 2, 6; Specification pages 16-17.	At least one of the first and second conductive layers is electrically connected to at least one of the source, drain, and gate electrodes of a thin film transistor. <u>Intrinsic Support</u> E.g., Figs. 3, 4, & 5; 4:46-5:53; 5:23-53 App 08/781,188, 12/01/97 Response, pg. 1-7

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
one of said first and second conductive layers	C	one, but not both, of the first and second conductive layers <u>Intrinsic Support</u> 4:46-5:23; Fig 3; App. No. 08/781,188, 12/1/1997, Amendment, at p. 5-7.	this term should be construed as part of the larger term "one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor"	At least one of the first and second conductive layers <u>Intrinsic Support</u> E.g., Figs. 3, 4, & 5; 4:46-5:53; 5:23-53 App 08/781,188, 12/01/97 Response, pg. 1-7
one	L	a single layer <u>Intrinsic Support</u> 4:46-5:23; Fig 3; App. No. 08/781,188, 12/1/1997, Amendment, at p. 5-7.	this term should be construed as part of the larger term "one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor"	Plain meaning <u>Intrinsic Support</u> E.g., Figs. 3, 4, & 5; 4:46-5:53; 5:23-53 App 08/781,188, 12/01/97 Response, pg. 1-7
connected to	C A	directly connected to <u>Intrinsic Support</u> 1:24-30; 2:31-3:15; 3:63-4:5; 4:46-5:23; Fig 3; App. No. 08/781,188, 12/1/1997, Amendment, at p. 5-7.	plain meaning	Electrically connected to <u>Intrinsic Support</u> E.g., Figs. 3, 4 & 5; 4:46-5:53; 5:23-53

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
one of a plurality of terminals of a thin film transistor	L	<p>one of the terminals (i.e., source, drain, or gate) of a thin film transistor</p> <p><u>Intrinsic Support</u></p> <p>4:46-5:23; Fig 3; App. No. 08/781,188, 12/1/1997, Amendment, at p. 5-7.</p>	<p>this term should be construed as part of the larger term "one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor"</p>	<p>At least one of the source, gate, and drain electrodes of a thin film transistor</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 4:46-5:53; 5:23-53 App 08/781,188, 12/01/97 Response, pg. 1-7</p>
a plurality of terminals of a thin film transistor	C	<p>the terminals (i.e., source, drain, or gate) of a thin film transistor</p> <p><u>Intrinsic Support</u></p> <p>4:46-5:23; Fig 3; App. No. 08/781,188, 12/1/1997, Amendment, at p. 5-7.</p>	<p>this term should be construed as part of the larger term "one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor"</p> <p>to the extent that the embedded term "terminals of a thin film transistor" needs to be construed, CMO proposes the following construction:</p> <p>the gate, source, and drain of a thin film transistor</p> <p>'449 File history, 12/1/1997 Amendment & Response, page 5</p>	<p>Source, drain, and gate electrodes of a thin film transistor</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 4:46-5:53; 5:23-53 App 08/781,188, 12/01/97 Response, pg. 1-7</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
thin film transistor	C	<p>A three terminal device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than in a single crystal silicon wafer</p> <p><u>Intrinsic Support</u></p> <p>1:22-33; Figs 1-3; App. No. 08/781,188, 12/1/1997, Amendment, at p. 5-7.</p>	<p>A three terminal semi-conductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semi-conductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than in a single crystal silicon wafer.</p> <p><u>Intrinsic Support</u></p> <p>1:13-30; Figs. 1f, 2e, 3, 4; 5/5/05 Order re Claim Construction, Case No. 02-6775, at 13; Second Revised Joint Claim Construction Statement, Case No. 02-6775, at 157-159; '449 Prosecution History, 12/1/1997 Amendment & Response, page 5</p>	<p>A three-terminal semiconductor device in which the current flow through one pair of , electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
liquid crystal display device	C	<p>a type of display that generates an image by directing light through an array of liquid crystal pixels, where the amount of light effused by each pixel is controlled via an electric field varying the orientation of the liquid crystal molecules contained within the pixel</p> <p><u>Intrinsic Support</u></p> <p>1:8-25; 1:31-34; Fig. 1-3.</p>	<p>a type of display that generates an image by directing light through an array of liquid crystal pixels, where the amount of light effused by each pixel is controlled via an electric field varying the orientation of the liquid crystal molecules contained within the pixel</p> <p><u>Intrinsic Support</u></p> <p>1:13-30; Fig. 6</p>	Plain meaning
gate electrode	C A	<p>a patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>1:22-38; 5:6-60; 2:37-44; 2:56-61; 3:44-49; 4:47-53; 4:65-5:1; 5:29-38; Figs. 1-3.</p>	<p>a patterned, electrically conductive material that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>Figs. 1a, 1e, 2a, 2e, 3 (e.g., element 2); 3:44-49; see also 1:34-37; 2:37-44; 2:56 - 3:1; 5:29-38.</p>	<p>A patterned, electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode</p> <p><u>Intrinsic Support</u></p> <p>E.g., Fig. 3; 2:37-3;14 (Summary of the Invention)</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
gate pad	C A	<p>a portion of patterned electrically conductive material that is provided near the periphery of the thin film transistor array to receive a gate signal</p> <p><u>Intrinsic Support</u></p> <p>1:22-38; 1:52-60; 2:8-10; 2:19-26; 3:44-49; 4:6-15; 4:21-27; 4:35-41; 4:47-53; 4:65-5:1; 5:19-23; Figs. 1, 3.</p>	<p>a portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive a gate signal from a gate driving circuit</p> <p><u>Intrinsic Support</u></p> <p>Figs. 1a-1e, 2a-2e (e.g., element 2C), 3 (e.g., element 2B), 6; 1:27-30; 1:34-38; 1:52-55; 2:39-40; 2:59-61; 4:8-15; 4:47-53; 4:65-5:1.</p> <p>5/5/05 Order re Claim Construction, Case No. 02 6775, at 17; Second Revised Joint Claim Construction Statement, Case No. 02 6775, at 162-165.</p>	<p>a patterned, electrically, conductive material that is provided near the periphery of the thin film transistor array to receive a gate signal from a gate driving circuit</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 4:65-5:5; 5:23-38; 5:39-54</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
source pad	L C A	<p>a portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive a data signal</p> <p><u>Intrinsic Support</u></p> <p>1:8-12; 1:22-38; 1:52-64; 2:8-10; 2:17-22; 3:66-4:5; 4:6-14; 4:24-27; 4:35-61; 4:65-5:1; 5:19-23; 5:48-51; Figs. 1-3.</p>	<p>a portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive a data signal from a data driving circuit</p> <p><u>Intrinsic Support</u></p> <p>Figs. 1a-1e, 2a-2e, 3 (e.g., element 2A), 6; 1:27-30; 1:34-38; 1:52-55; 1:67 – 2:4; 4:8-15.</p> <p>5/5/05 Order re Claim Construction, Case No. 02 6775, at 17; Second Revised Joint Claim Construction Statement, Case No. 02 6775, at 165-168..</p>	<p>a patterned, electrically, conductive material that is provided near the periphery of the thin film transistor array to receive a data signal from a data driving circuit</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 4:65-5:5; 5:23-38; 5:39-54</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
a gate insulating film on said surface of said substrate	C	<p>a thickness of non-conductive material (such as SiNx) that has high electrical resistance and insulates the transistor gate from the semiconductor above and in contact with at least part of the surface of the substrate</p> <p><u>Intrinsic Support</u></p> <p>1:52-55; 2:11-13; 2:19-26; 2:34-36; 2:40-44; 3:50-53; 4:1-15; 4:35-39; 4:47-50; 4:65-5:4; 5:12-15; 5:19-23; 5:40-46; Figs. 1-3.</p>	plain meaning	<p>A gate insulating film above, supported by, and in contact with the surface of the substrate</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 4:65-5:5; 5:23-38; 5:39-54</p>
gate insulating film	C	<p>a thickness of non-conductive material (such as SiNx) that has high electrical resistance and insulates the transistor gate from the semiconductor</p> <p><u>Intrinsic Support</u></p> <p>1:52-55; 2:11-13; 2:19-26; 2:34-36; 2:40-44; 3:50-53; 4:1-15; 4:35-39; 4:47-50; 4:65-5:4; 5:12-15; 5:19-23; 5:40-46; Figs. 1-3.</p>	plain meaning	<p>Plain meaning:</p> <p>or</p> <p>Insulating film formed over the gate region</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 4:65-5:5; 5:23-38; 5:39-54</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
insulating film	C	<p>a thickness of non-conductive material (such as SiNx) that has high electrical resistance</p> <p><u>Intrinsic Support</u></p> <p>1:52-55; 2:11-13; 2:19-26; 2:34-36; 2:40-44; 3:50-53; 4:1-15; 4:35-39; 4:47-50; 4:65-5:4; 5:12-15; 5:19-23; 5:40-46; Figs. 1-3.</p>		Plain meaning
a semiconductor layer on said portion of said gate insulating film	C	<p>a thickness of semiconductor material above and in contact with a part of the gate insulating film</p> <p><u>Intrinsic Support</u></p> <p>1:40-51; 1:61-2:4; 2:37-3:15; 3:50-4:5; 4:65-5:5; Figs 1-3.</p>	<p>a thickness of semiconductor material above and in contact with a part of the gate insulating film</p> <p><u>Intrinsic Support</u></p> <p>Figs. 1b-1f, 2b-2e, 3; 1:53-54, 2:42-44; 2:61-64; 3:50-62; 5:1-5</p>	<p>A semiconductor above, supported by, and in contact with the portion of the gate insulating film</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 4:65-5:5; 5:23-38; 5:39-54</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
semiconductor layer	C	<p>a thickness of semiconductor material, such as amorphous silicon</p> <p><u>Intrinsic Support</u></p> <p>1:40-51; 1:61-2:4; 2:37-3:15; 3:50-4:5; 4:65-5:5; Figs 1-3.</p>	<p>a thickness of a semiconductor material, such as amorphous silicon</p> <p><u>Intrinsic Support</u></p> <p>1:53-54, 2:42-44; 5:1-5; Figs. 1b – 1f, 2b – 2e, 3</p>	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 4:65-5:5; 5:23-38; 5:39-54</p>
impurity-doped semiconductor layer	C	<p>a thickness of semiconductor material, such as amorphous silicon, to which impurities (such as phosphorous atoms) have been added to enhance electrical conductivity</p> <p><u>Intrinsic Support</u></p> <p>1:40-51; 1:61-2:4; 2:37-3:15; 3:50-4:5; 4:65-5:5; Figs 1-3.</p>	<p>a thickness of semiconductor material, such as amorphous silicon, to which impurities (such as phosphorous atoms) have been added to enhance electrical conductivity</p> <p><u>Intrinsic Support</u></p> <p>1:43-48, 3:52-63; 5:1-5; Figs. 2b – 2e, 3 (e.g., element 5)</p>	<p>Plain meaning;</p> <p>or</p> <p>Semiconductor layer doped with impurities</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 4:65-5:5; 5:23-38; 5:39-54</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
a source electrode and a drain electrode on said semiconductor layer	A	<p>a source electrode and a drain electrode above and in contact with the semiconductor layer</p> <p><u>Intrinsic Support</u></p> <p>1:40-51; 1:61-2:4; 2:37-3:15; 3:50-4:5; 4:65-5:15; Figs 1-3.</p>	<p>a source electrode and a drain electrode above and in contact with the semiconductor layer</p> <p><u>Intrinsic Support</u></p> <p>Figs. 1e-1f, 2c-2e, 3 (e.g., source electrode 7 and drain electrode 8)</p> <p>1:44-50; 1:61-67; 3:56-60; 3:63-66; 4:27-34; 5:6-8</p>	<p>The source electrode and the drain electrode above, supported by, and in contact with the semiconductor layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 5:6-5:15; 5:23-38; 5:39-54</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
source electrode	C A	<p>a patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode</p> <p><u>Intrinsic Support</u></p> <p>1:8-12; 1:22-30; 1:61-2:4; 2:11-27; 2:37-3:15; 3:63-4:5; 4:47-64; 5:6-22; 5:29-39; 5:48-54; Figs. 1e-1f; 2c-e, 3.</p>	<p>Construe term:</p> <p>"a source electrode and a drain electrode"</p> <p>as:</p> <p>Patterned, electrically conductive material formed over the source region and drain region, respectively, of a transistor. Current flows through the channel between the source electrode and the drain electrode of the transistor under control of the gate electrode of the transistor.</p> <p><u>Intrinsic Support</u></p> <p>Figs. 1e-1f, 2c-2e, 3 (e.g., source electrode 7 and drain electrode 8); 1:44-50; 1:61-67; 3:56-60; 3:63-66; 4:27-34; 5:6-8</p>	<p>A patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 5:6-5:15; 5:23-38; 5:39-54</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
drain electrode	C A	<p>a patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source and drain electrode under the control of the gate electrode</p> <p><u>Intrinsic Support</u></p> <p>1:8-12; 1:22-30; 1:61-2:4; 2:11-27; 2:37-3:15; 3:63-4:5; 4:47-64; 5:6-22; Figs. 1e-1f; 2c-e, 3.</p>	<p>this term should be construed as part of the larger term "a source electrode and a drain electrode" (see above)</p>	<p>A patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 5:6-5:15; 5:23-38; 5:39-54</p>
passivation layer	C	<p>a thickness of insulative material that provides protection such as electrical stability and chemical isolation</p> <p><u>Intrinsic Support</u></p> <p>2:5-10; 2:19-26; 2:34-36; 2:40-46; 3:50-53; 4:1-15; 4:35-39; 4:47-50; 4:65-5:4; 5:12-15; 5:19-23; 5:40-46; Figs. 1-3.</p>	<p>a thickness of insulative material that provides protection such as electrical stability and chemical isolation</p> <p><u>Intrinsic Support</u></p> <p>Figs. 1f, 2d-2e, 3 (e.g, element 9); 2:5-8; 4:6-8; 5:6-15</p>	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 5:6-5:15; 5:23-38; 5:39-54</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
exposing said gate pad portion	A	removing portions of one or more layers to uncover at least part of a gate pad [portion] <u>Intrinsic Support</u> 1:52-60; 2:5-10, 17-28, 45-55; 3:1-14, 3:66-4:15; 4:35-65; 5:6-22; Abstract; Figs 1-3.	plain meaning	Causing the gate pad to be exposed to the atmosphere <u>Intrinsic Support</u> E.g., Figs. 3, 4, & 5; 2:37-3:14 (Summary of the Invention); 4:46-5:22
exposing	C	removing portions of one or more layers to uncover at least part of another layer <u>Intrinsic Support</u> 1:52-60; 2:5-10, 17-28, 45-55; 3:1-14, 3:66-4:15; 4:35-65; 5:6-22; Abstract; Figs 1-3.	plain meaning	Laying open or causing to be exposed from above <u>Intrinsic Support</u> E.g., Figs. 3, 4, & 5; 4:46-5:53; 5:23-53

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
pixel electrode	C	<p>a pattern of transparent electrically conductive material that stores charge to drive the liquid crystal material within an individual element of the liquid crystal display device</p> <p><u>Intrinsic Support</u></p> <p>1:24-30; 1:56-2:4; 2:16-28; 2:31-3:15; 3:16-41; 4:54-64; 5:15-22; Figs 1-3.</p>	<p>electrode controlling the brightness of a pixel</p> <p><u>Intrinsic Support</u></p> <p>1:15-19, 1:26-30, 1:56-59, 1:67-2:4</p>	<p>Electrode controlling the brightness of a pixel</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 4:46-4:64; 5:16-23; 5:39-54</p>
transparent conductive layer	C	<p>a thickness of transparent electrically conductive material</p> <p><u>Intrinsic Support</u></p> <p>1:55-60; 4:16-19; 4:39-41; 5:15-22; Figs 1-3.</p>	plain meaning	Plain meaning
a method of manufacturing a liquid crystal display device	C	<p>a process for producing a liquid crystal display device</p> <p><u>Intrinsic Support</u></p> <p>1:8-25; 1:31-34; Fig. 103.</p>	plain meaning	Plain meaning

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
patterning ... to form an active layer	C	<p>the removal of selected portions of the impurity-doped semiconductor layer and the semiconductor layer using etching techniques in order to form an active layer</p> <p><u>Intrinsic Support</u></p> <p>1:34-37; 1:44-50; 1:55-67; 2:16-28; 2:56-3:14; 3:44-4:5; 4:16-24; 4:47-5:22; Figs 1-3.</p>	plain meaning	<p>selectively removing portions of ... using etching techniques in order to form an active region</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 4:46-4:64; 4:65-5:5; 5:23-53</p>
patterning	C	<p>the removal of selected portions of a surface using etching techniques in order to produce a pattern in the remaining material</p> <p><u>Intrinsic Support</u></p> <p>1:34-37; 1:44-50; 1:55-67; 2:16-28; 2:56-3:14; 3:44-4:5; 4:16-24; 4:47-5:22; Figs 1-3.</p>	plain meaning	<p>selectively removing portions of a surface using etching techniques in order to produce a pattern in the remaining material</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 4:46-4:64; 4:65-5:5; 5:23-53</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
active layer	C A	<p>a discrete portion of semiconductor layer that is formed by patterning and located at least in part above the gate electrode. In operation, the discrete portion is penetrated, at least in part, by the electric field introduced by the gate electrode.</p> <p><u>Intrinsic Support</u></p> <p>1:34-51; 1:61-2:4; 2:11-27; 3:44-62; 4:65-5:5; 5:39-47; Figs 1-3.</p>	<p>A discrete portion of the semiconductor layer that is formed by patterning and located along the gate electrode of a thin film transistor. In operation, the discrete portion is penetrated, at least in part, by the electric field introduced by the gate electrode of the thin film transistor.</p> <p><u>Intrinsic Support</u></p> <p>1:42-44; 3:47-49; 3:50-62; 5:1-5</p> <p>5/5/05 Order re Claim Construction, Case No. 02 6775, at 18; Second Revised Joint Claim Construction Statement, Case No. 02 6775, at 176-177.</p>	<p>active region of a thin film transistor</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 4:46-4:64; 4:65-5:5; 5:23-53</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
selectively etching	C	<p>the removing selected portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) in order to produce a desired pattern on the surface</p> <p><u>Intrinsic Support</u></p> <p>1:47-55; 2:8-10; 2:31-36; 2:50-51; 3:59-61; 3:67-4:1; 4:8-19; 4:35-39; 4:47-50; 5:1-15; 5:40-47; Figs 1-3.</p>	plain meaning	<p>selectively removing portions of a surface using etching techniques in order to produce a desired pattern in the remaining material</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, & 5; 4:46-5:53</p>
patterning a pixel electrode electrically connected to said drain electrode	C	<p>the removal of selected portions of a pattern of transparent electrically conductive material to form a pixel electrode that has an electrical conduction path with the drain electrode</p> <p><u>Intrinsic Support</u></p> <p>1:34-37; 1:44-50; 1:55-67; 2:16-28; 2:56-3:14; 3:44-4:5; 4:16-24; 4:47-5:22; Figs 1-3.</p>	plain meaning	<p>selectively removing portions of a pixel electrode using etching techniques in order to electrically connect the pixel electrode to the drain electrode</p> <p><u>Intrinsic Support</u></p> <p>E.g., , Figs. 3, 4, & 5; 4:46-5:53</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
electrically connect/electrically connecting/electrically connected	A	provide an electrical conduction path <u>Intrinsic Support</u> 1:24-30; 2:31-3:15; 4:56-64; 5:8-22; Figs 1-3.	plain meaning	Plain meaning

EXHIBIT D

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Claim Terms	Des.	Agreed Constructions
drain electrode	A	A patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.
source electrode	A	A patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.

Disputed Constructions

Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
the gate line having an opening therein	A	<p>the gate line has a space in its pattern to reduce gate-drain capacitance and compensate for gate-drain layer misalignment</p> <p><u>Intrinsic Support</u></p> <p>1:13-16; 1:67-2:11; 2:23-67; 3:2-6; 3:30-48; 4:6-11; 4:20-40; 4:47-5:2; 5:41-6:17; 6:21-41; 7:40-57; 7:60-8:28; 8:36-9:17; Abstract; Figs. 4-9; App. No. 09/867,484, 03/13/3003, Office Action; pages 3-4; App. No. 09/867,484, 5/6/2003, Interview Summary; App. No. 09/867,484, 5/8/2002, Response, page 10-11.</p>		<p>Gate line with a cut out extending from the periphery of the gate line to the interior of the gate line</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 5-8; Abstract;; 4:63-65; 6:13-15; 6:31-41; 8:7-10; 8:37-42; 7:6-17; 7:41-43; App 09/867484, 5/12/03, Response, pages 10-11</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
a gate line	L	<p>a pattern of electrically conductive material that conveys gate signals to transistors, a portion of which controls current flow through the channel between the source and drain electrodes</p> <p><u>Intrinsic Support</u></p> <p>1:67-2:11; 2:23-35; 2:63-67; 3:2-6; 3:30-48; 5:41-6:17; 6:21-41; 7:60-8:4; 8:36-42; 8:63-9:17; Abstract; Figs. 4-9; App. No. 09/867,484, 03/13/3003, Office Action; pages 3-4; App. No. 09/867,484, 5/6/2003, Interview Summary; App. No. 09/867,484, 5/8/2002, Response, page 10-11.</p>		<p>An elongated directional conductor that supplies signals to gate electrodes</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 1, 2, 7, 8; 2:23-25; 5:40-53; 8:37-42; 1:65-2:8; 2:63-65</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
having an opening therein	L	<p>has a space in its pattern to reduce gate-drain capacitance and compensate for gate-drain layer misalignment</p> <p><u>Intrinsic Support</u></p> <p>1:13-16; 2:23-3:67; 4:6-11; 4:20-40; 4:47-5:2; 5:47-57; 5:66- 6:17; 6:28-41; 7:40-57; 8:2-28; 8:41-9:17; Abstract; Figs. 5-9; App. No. 09/867,484, 03/13/3003, Office Action; pages 3-4; App. No. 09/867,484, 5/6/2003, Interview Summary; App. No. 09/867,484, 5/8/2002, Response, page 10-11.</p>		<p>Having a cut out extending from the periphery to a point within</p> <p><u>Intrinsic Support</u></p> <p>See support for limitation "the gate line having an opening therein"</p>
a semiconductor layer on the first insulating layer over at least a portion of the opening	A	<p>a layer of semiconductor material, above and supported by or in contact with the first insulating layer, a portion of which overlaps part of the space in the gate line</p> <p><u>Intrinsic Support</u></p> <p>4:30-40; 6:29-58; 7:6-24; 8:1-13; Fig. 4-9; Abstract.</p>		<p>A semiconductor layer above, supported by, and in contact with the first insulating layer, the semiconductor layer being over at least a portion of the opening in the gate line</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 6A, 8 and 9; 6:47-54</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
a drain electrode on the semiconductor layer over at least a portion of the opening	A	<p>a drain electrode, above and supported by or in contact with the semiconductor layer, a portion of which overlaps part of the space in the gate line</p> <p><u>Intrinsic Support</u></p> <p>2:6-11; 2:24-3:29; 3:36-40; 3:48-67; 4:9-11; 4:32-40; 4:48-65; 5:54-6:17; 6:64-7:23; 7:41-8:28; 8:37-9:17; Figs. 4, 6b, 6c-9; Abstract .</p>		<p>A drain electrode above, supported by, and in contact with the semiconductor layer, the drain electrode being over at least a portion of the opening in the gate line</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 6A, 8 and 9, 7:48-51; 7:6-20</p>
pixel electrode	A	<p>a pattern of transparent electrically conductive material that stores charge to drive the liquid crystal material within an individual element of the liquid crystal display device</p> <p><u>Intrinsic Support</u></p> <p>1:37-65; 2:13-22; 7:33-39; Fig 1, 2, 9.</p>		<p>Electrode controlling the brightness of a pixel</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 1-5, 6B-6C, 7-9; 1:38-48; 2:13-22; 2:24-39; 4:43-36; 6:61-63; 7:34-40</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
substantially surrounds the drain electrode	A	extending considerably around a portion of the drain electrode <u>Intrinsic Support</u> 4:20-40; 5:59-65; 6:66-7:7:5; 8:5-10; Abstract; Fig. 5, 6B, 6C, 7, 8.		Surrounds almost all the drain electrode portion <u>Intrinsic Support</u> E.g., Figs. 5 6B, 6C; 4:37-40; 5:53-61; 6:66-7:2; 7:18-23; 8:5-7.
substantially	A	considerably <u>Intrinsic Support</u> 4:20-40; 5:59-65; 6:66-7:7:5; 8:5-10; Abstract; Fig. 5, 6B, 6C, 7, 8.		Almost all <u>Intrinsic Support</u> E.g., Figs. 5 6B, 6C, 4:37-40; 5:53-61; 6:66-7:2; 7:18-23; 8:5-7.

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
the gate electrode having an opening therein	A	<p>the gate electrode has a space in its pattern to reduce gate-drain capacitance and compensate for gate-drain layer misalignment</p> <p><u>Intrinsic Support</u></p> <p>1:13-16; 1:67-2:11; 2:23-67; 3:2-6; 3:30-48; 4:6-11; 4:20-40; 4:47-5:2; 5:41-6:17; 6:21-41; 7:40-57; 7:60-8:28; 8:36-9:17; Abstract; Figs. 4-9; App. No. 09/867,484, 03/13/3003, Office Action; pages 3-4; App. No. 09/867,484, 5/6/2003, Interview Summary; App. No. 09/867,484, 5/8/2002, Response, page 10-11.</p>		<p>gate electrode with a cut out extending from the periphery of the gate, line to the interior of the gate line</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 5-8; Abstract; 6:31-41; 8:37-42; Abstract; 4:63-65; 8:7-10; 6:13-15; 7:6-17; 7: 41-43</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
gate electrode	L A	<p>patterned electrically conductive material that includes a portion that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>1:67-2:11; 2:23-35; 2:63-67; 3:2-6; 3:30-48; 5:41-6:17; 6:21-41; 7:60-8:4; 8:36-42; 8:63-9:17; Abstract; Figs. 4-9; App. No. 09/867,484, 03/13/3003, Office Action; pages 3-4; App. No. 09/867,484, 5/6/2003, Interview Summary; App. No. 09/867,484, 5/8/2002, Response, page 10-11.</p>		<p>A patterned, electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-5; 8:64-65; 3:30-40; 4:27-31; 6:27-32. App 09/867484, 5/12/03 Response, pages 10-11</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
the opening includes a first opening portion and a second opening portion	A	<p>the space in the gate electrode pattern includes a first part to primarily compensate for gate-drain layer misalignment and a second part to primarily reduce gate-drain capacitance</p> <p><u>Intrinsic Support</u></p> <p>1:13-16; 2:23-3:67; 4:6-11; 4:20-40; 4:47-5:2; 5:47-57; 5:66- 6:17; 6:28-41; 7:40-57; 8:2-28; 8:41-9:17; Abstract; Figs. 5-9; App. No. 09/867,484, 03/13/3003, Office Action; pages 3-4; App. No. 09/867,484, 5/6/2003, Interview Summary; App. No. 09/867,484, 5/8/2002, Response, page 10-11.</p>		<p>Non-rectangular-shaped opening having two distinct opening portions</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 6A, 6B, 9; Abstract; 4:48-50; 6:32-41; 7:17-18</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
a first opening portion	L	<p>a first part to primarily compensate for gate-drain layer misalignment</p> <p><u>Intrinsic Support</u></p> <p>1:13-16; 2:23-3:67; 4:6-11; 4:20-40; 4:47-5:2; 5:47-57; 5:66- 6:17; 6:28-41; 7:40-57; 8:2-28; 8:41-9:17; Abstract; Figs. 5-9; App. No. 09/867,484, 03/13/3003, Office Action; pages 3-4; App. No. 09/867,484, 5/6/2003, Interview Summary; App. No. 09/867,484, 5/8/2002, Response, page 10-11.</p>		<p>One distinct opening portion</p> <p><u>Intrinsic Support</u></p> <p>See above</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
a second opening portion	L	<p>a second part to primarily reduce gate-drain capacitance</p> <p><u>Intrinsic Support</u></p> <p>1:13-16; 2:23-3:67; 4:6-11; 4:20-40; 4:47-5:2; 5:47-57; 5:66- 6:17; 6:28-41; 7:40-57; 8:2-28; 8:41-9:17; Abstract; Figs. 5-9; App. No. 09/867,484, 03/13/3003, Office Action; pages 3-4; App. No. 09/867,484, 5/6/2003, Interview Summary; App. No. 09/867,484, 5/8/2002, Response, page 10-11.</p>		<p>Another distinct opening portion</p> <p><u>Intrinsic Support</u></p> <p>See above</p>
a first electrode	L	<p>a first portion of the drain electrode to primarily compensate for gate-drain layer misalignment</p> <p><u>Intrinsic Support</u></p> <p>4:48-5:2; 5:4-6:17; 7:6-23; 7:41-59; 8:7-28; 8:34-9:17; Abstract; Figs. 2-925-31, 35-37.</p>		<p>One distinct portion of a single electrode</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 5, 6B, 6C, 7-9; 4:53-60; 7:6-17; 6:6-12</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
a second electrode	L	<p>a second portion of the drain electrode to primarily reduce gate-drain capacitance</p> <p><u>Intrinsic Support</u></p> <p>4:48-5:2; 5:4-6:17; 7:6-23; 7:41-59; 8:7-28; 8:34-9:17; Abstract; Figs. 2-925-31, 35-37.</p>		<p>Another distinct portion of a single electrode</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 5, 6B, 6C, 7-9; 4:53-60; 7:6-17; 6:6-12</p>
a third electrode	L	<p>a third portion of the drain electrode to primarily connect to the pixel electrode</p> <p><u>Intrinsic Support</u></p> <p>2:13-22; 4:41-47; 7:24-39; Abstract; Figs. 2-5, 6B, 6C, 7-9.</p>		<p>The third distinct portion of the single electrode</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 5, 6B, 6C, 7, 8; 5:61-65; 7:29-32</p>
connects	L	<p>joins</p> <p><u>Intrinsic Support</u></p> <p>2:13-22; 4:41-47; 5:61-65; 7:24-39; Figs. 2-5, 6B, 6C, 7-8.</p>		<p>Physically attached</p> <p><u>Intrinsic Support</u></p> <p>E.g., 5, 6B, 6C, 7, 8, 5:57-65</p>

EXHIBIT E

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Disputed Constructions

Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
a first substrate	C	<p>one of a TFT or color filter substrate</p> <p><u>Intrinsic Support</u></p> <p>5:11-22; 7:9-13; Figs. 2, 3, and 4.</p>	<p>plain meaning</p> <p><u>Intrinsic Support</u></p> <p>Abstract, 3:61-65, 5:11-25, 7:17-34, Figs. 2-4</p>	<p>Plain meaning;</p> <p>or</p> <p>one of the two opposing substrates of the liquid crystal cell</p> <p><u>Intrinsic Support</u></p> <p>E.g., 1:38-39, 1:59-61; 7:25-33; Claim 5 and 9</p>
a second substrate	C	<p>the other of the TFT or color filter substrate</p> <p><u>Intrinsic Support</u></p> <p>5:11-22; 7:9-13; Figs. 2, 3, and 4.</p>	<p>The substrate immediately following the first substrate</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 3:61-66; 5:11-25; 7:17-34; Figs. 2-4</p>	<p>Plain meaning</p> <p>or</p> <p>the other of the two opposing substrates of the liquid crystal cell</p> <p><u>Intrinsic Support</u></p> <p>See above</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
on a single production process line	L	<p>on a production line where the processing equipment is arranged along a common path for performing the liquid crystal cell processes</p> <p><u>Intrinsic Support</u></p> <p>3:25-42; 5:23-30; 7:9-13, 35-41; Figs. 2, 3, and 4; App 10/124,452, 6/17/04 Notice of Allowability, pages 2-3.</p>	<p>On a line structure for processing the substrates in only one direction without branching</p> <p><u>Intrinsic Support</u></p> <p>Abstract, 3:22-53; 3:61-4:13, 5:23-30, 7:17-43, Figs. 1-4, App. No. 10/128,452, January 6, 2004 Amendment at 4-5</p>	<p>On a production line for processing liquid crystal displays in a single, linear arrangement</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-4; 5:23-27; 7:35-43; Claim 1; App 10/128452, 1/8/04 Amendment</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
passing the first and second substrates through a sealing material coating portion of the single production process line in serial order	C	<p>passing the first and second substrates, one after the other, along a portion of the single production process line where the sealing material is selectively applied</p> <p><u>Intrinsic Support</u></p> <p>3:25-42; 5:11-30, 39-50, 62-6; 6:27-34, 42-6; 7:1-13, 35-41; Figs. 2, 3, and 4; App 10/124,452, 6/17/04 Notice of Allowability, pages 2-3.</p>	<p>Providing the first and second substrates, one after the other without anything in between, in at one end, and out at the other end, of a machine for coating sealing material in the single production process line in which the same order of the first and second substrates is maintained throughout the seal dispensing process</p> <p><u>Intrinsic Support</u></p> <p>Abstract, 2:28-38, 2:54-59, 3:61-4:13; 5:11-30, 5:39-50, 6:27-34, 7:1-8, 7:17-44, Figs. 2-4, App. No. 10/128,452, January 6, 2004 Amendment at 4-5</p>	<p>providing the first and second substrate one after the other, without anything in between; in at one end, and out at the other end in the same order of a machine for coating sealing material on a substrate</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-4; 4:20-25, 5:23-30; 6:19-53; 6:54-7:20; App 10/128452, 1/8/04 Amendment, pages 1-6; App 10/128452, 6/23/04</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
a sealing material coating portion of the single production process line	A	<p>a portion of the single production process line where the sealing material is selectively applied</p> <p><u>Intrinsic Support</u></p> <p>3:25-42; 5:11-30; 5:39-50; 5:62-66; 6:27-34; 6:42-6; 7:1-13; 7:35-41; Figs. 2, 3, and 4.</p>	<p>a machine for coating sealing material in the single production process line</p> <p><u>Intrinsic Support</u></p> <p>Abstract, 2:28-38, 2:54-59, 3:61-4:13, 5:11-30, 5:39-50, 6:27-34, 7:1-8, 7:17-44, Figs. 2-4, App. No. 10/128,452, January 6, 2004 Amendment at 4-5</p>	<p>A machine for coating sealing material in the single production process line.</p> <p><u>Intrinsic Support</u></p> <p>See above</p>
in serial order	A	<p>one after the other</p> <p><u>Intrinsic Support</u></p> <p>5: 39-50, 55-66; 6:27-46, 62-7; 7:1-13, 21-3.</p>	<p>one after the other one without anything in between</p> <p><u>Intrinsic Support</u></p> <p>Abstract, 3:61-4:13, 5:11-25, 5:41-49, 5:56-61, 6:27-41, 6:62-67, 7:1-8, 7:17-34, Figs. 2-4, App. No. 10/128,452, January 6, 2004 Amendment at 4-5</p>	<p>One after the other without anything in between</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-4; 5:23-27; 7:25-33; 6:19-53 & Fig. 3; 6:54-7:20 & Fig. 4</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
passing the first and second substrates through a liquid crystal dispensing portion of the single production process line in serial order	C	<p>passing the first and second substrates, one after the other, along a portion of the single production process line where liquid crystal is selectively dispensed</p> <p><u>Intrinsic Support</u></p> <p>3:25-42; 5:11-30, 55-66 6:35-46; 6:62-67; 7:9-13; 7:35-41; Figs. 2, 3, and 4; App 10/124,452, 6/17/04 Notice of Allowability, pages 2-3.</p>	<p>providing the first and second substrates, one after the other without anything in between, in at one end, and out at the other end, of a machine for dispensing liquid crystal material in the single production process line in which the same order of the first and second substrates is maintained throughout the liquid crystal dispensing process</p> <p><u>Intrinsic Support</u></p> <p>Abstract, 2:28-38, 2:63-3:12, 3:61-4:13, 5:11-30, 5:56-61, 6:36-41, 6:62-67, 7:17-34, Figs. 2-4, App. No.10/128,452, January 6, 2004 Amendment at 4-5</p>	<p>providing the first and second substrate one after the other, without anything in between; in at one end, and out at the other end in the same order of the liquid crystal dispensing machine</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-4; 4:26-30; 6:19-53; 6:54-7:20; App 10/128452, 1/8/04 Amendment, pages 1-6 App 10/128452, 6/23/04 Notice of Allowability, pages 1-4</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
a liquid crystal dispensing portion of the single production process line	A	<p>a portion of the single production process line where liquid crystal is selectively dispensed</p> <p><u>Intrinsic Support</u></p> <p>3:25-42; 5:11-30; 5:55-66; 6:35-46; 6:62-67; 7:9-13; 7:35-41; Figs. 2, 3, and 4; App 10/124,452, 6/17/04 Notice of Allowability, pages 2-3.</p>	<p>a machine for dispensing liquid crystal in the single production process line</p> <p><u>Intrinsic Support</u></p> <p>Abstract, 2:28-38, 2:63-3:12, 3:61-4:13, 5:11-30, 5:56-61, 6:36-41, 6:62-67, 7:17-34, Figs. 2-4, App. No. 10/128,452, January 6, 2004 Amendment at 4-5</p>	<p>a machine for dispensing liquid crystal on a substrate in the single production process line</p> <p><u>Intrinsic Support</u></p> <p>See above</p>
a pixel region	C	<p>area corresponding to the inside of the sealing material</p> <p><u>Intrinsic Support</u></p> <p>5:40-66; 6:27-46; 6:62-7:13.</p>	<p>an area with pixels</p> <p><u>Intrinsic Support</u></p> <p>2:45-53, 3:6-12, 4:7-11, 5:39-47, 6:27-33; 7:1-5</p>	<p>Area with pixel</p> <p><u>Intrinsic Support</u></p> <p>E.g., 2:48-40; 5:16-18; Claim 7</p>
assembling	C	<p>bringing together</p> <p><u>Intrinsic Support</u></p> <p>1:57-61; 3:13-6; 5:44-7; 6:50-2; Figs. 1, 2, 3, and 4.</p>	Indefinite	Indefinite

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
the liquid crystal is dispensed onto the first substrate at the same time that the second substrate is disposed in the sealing material coating portion	A	a point in time when liquid crystal is being dispensed on the first substrate overlaps with a point in time when the second substrate is located in the portion of the single production process line where the sealing material is selectively applied <u>Intrinsic Support</u> 7:22-34.	when the liquid crystal is dispensed onto the first substrate in the machine for dispensing liquid crystal, the second substrate is located in the machine for coating sealing material <u>Intrinsic Support</u> 7:21-34, Figs. 3-4	when the liquid crystal is dispensed onto the first substrate in the liquid crystal dispensing machine, the second substrate is located in the sealant coating machine <u>Intrinsic Support</u> E.g., 7:22-33
in serial order in a same cleaning unit	L	one after the other in the same cleaning equipment <u>Intrinsic Support</u> 3:25-42; 3:36-43; 5:26-30; 5:11-30, 55-66 6:35-46; 6:62-67; 7:9-13; 7:35-41; Figs. 2, 3, and 4.	one after the other without anything in between, in a same cleaning machine <u>Intrinsic Support</u> 3:22-42, 5:26-30, 5:33-38, 6:19-27, 6:54-61, Figs. 1-4	cleaning the first substrate and the second substrate one after the other without anything in between in the same cleaning machine <u>Intrinsic Support</u> E.g., Figs. 2-4; 5:23-36; 6:19-21; 6:54-56

EXHIBIT F

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Claim Terms	Des.	Agreed Constructions
substrate	C	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support

Disputed Constructions

Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
transistor	C	<p>a three terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer, and the thin film transistor is formed using thin-film techniques on a substrate</p> <p><u>Intrinsic Support</u></p> <p>1:5-20; 1:44-46; 2:49-51; 3:21-63; 5:38-41; Figs 1-4; Abstract.</p>	<p>a three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate</p> <p><u>Intrinsic Support</u></p> <p>1:15-16; 4:26-31; Fig. 2; Fig. 3</p>	<p>Plain meaning or A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate</p> <p><u>Intrinsic Support</u></p> <p>4:23-31; 4:39-44; 6:55-61; Claim 4</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
gate	L	<p>patterned electrically conductive material that includes a portion that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>1:5-39; 3:21-29; 3:41-64; 4:26-34; 4:40-5:7; 5:21-37; 5:63-6:7; 6:15-48; 7:7-52; Figs 1-4; Abstract.</p>	<p>A region of a transistor</p> <p><u>Intrinsic Support</u></p> <p>4:26-31; Fig. 2; Fig. 3</p>	<p>same as gate electrode; a patterned, electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.</p> <p><u>Intrinsic Support</u></p> <p>E.g., 4:26-5:3</p>
a double layered structure	C A	<p>a structure of an electrically conductive material that includes two sequentially deposited metal layers</p> <p><u>Intrinsic Support</u></p> <p>1:5-10; 1:20-43; 2:55-3:19; 3:27-64; 4:24-34; 4:40-62; 5:22-38; 5:42-62; 6:27-49; 7:32-52; Figs. 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment.</p>	<p>a structure having only two metal layers.</p> <p><u>Intrinsic Support</u></p> <p>1:17-23; 3:27-29; 4:32-34; 5:21-25; 6:27-29; Fig. 2; Fig. 3; Figs. 4A-F; Application, 08/918,119, Response, November 17, 1998</p>	<p>a two-layered step structure</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3-4; 1:20-2:65; 3:27-58; 4:23-59; 5:21-38; 6:27-48</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
a second metal layer disposed on the first metal layer	L C	<p>sequentially depositing the second metal layer above and in contact with the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>1:20-27; 2:49-3:20; 3:27-40; 3:45-58; 4:26-39; 4:53-59; 5:21-38; 5:42-54; 7:32-59; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment.</p>	<p>The second metal layer is in contact with the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>3:49-51; Abstract; Fig 3, Figs. 4A-F</p>	<p>a second metal layer precipitated above, supported by and in contact with the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., 5:41-54</p>
the first metal layer including aluminum	C	<p>the first metal layer containing aluminum and possibly other materials</p> <p><u>Intrinsic Support</u></p> <p>1:6-10; 1:17-26; 1:40-43; 1:51-55; 3:22-26; 4:32-38; 5:42-54; 7:47-52, App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment.</p>	Plain meaning	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>E.g., 4:34-36; 5:42-43; 1:17-22</p>
the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer	C	the second metal layer is patterned to prevent hillock on the side surfaces of the first metal layer that are	the second metal layer prevents hillock on the sides of the aluminum first metal layer	the second metal layer being arranged on the first metal layer to prevent hillocks from forming on the side

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
		<p>exposed to a subsequently deposited gate insulating layer</p> <p><u>Intrinsic Support</u></p> <p>1:17-43; 2:49-65; 3:21-29; 3:34-40; 5:21-38; 6:37-48; 7:47-52; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment.</p>	<p><u>Intrinsic Support</u></p> <p>1:20-38; 3:20-26; 6:40-47</p>	<p>portions of the aluminum first metal layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3-4; 1:20-2:65; 3:21-25; 4:46-55; 5:21-38; 6:27-48; App 08/918119, 11/17/98 Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance, page 2; App</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
				08/918462, 4/26/99 Office Action, pages, 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99, Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462, 4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9 10; App 09/983629, 8/8/01 Notice of Allowance, page 2
at the sides of the aluminum first metal layer	L C A	the side surfaces of the first metal layer that are exposed to a subsequently deposited gate insulating layer <u>Intrinsic Support</u> 1:17-43; 2:49-65; 3:21-29; 3:34-40; 5:21-38; 6:37-48; 7:47-52; Figs 1-4; Abstract;	Indefinite	at the portions on the top surface of the first metal layer not covered by the second metal layer <u>Intrinsic Support</u> E.g., Figs. 3-4; 4:23-59; 5:21-38; 6:45-47 App 08/918119, 11/17/98

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
		App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment.		Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance; page 2; App 08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462,

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
				4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9 10; App 09/983629, 8/8/01 Notice of Allowance, page 2

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
the first metal layer being wider than the second metal layer by about 1 to 4 μm	L C A	<p>the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more than 1 μm and less than 4 μm greater than the width of the second metal layer</p> <p><u>Intrinsic Support</u></p> <p>1:51-2:21; 3:41-64; 4:32-52; 5:21-38; 5:55-62; 5:67-6:48; 7:47-52; Abstract; Figs. 1-4; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment.</p>	<p>The top surface of the first metal layer has a width that is about 1 to 4 μm wider than a width of the top surface of the second metal layer to form a double step. A double step is a structure where not all of the top surface of the first metal layer is covered by the second metal layer.</p> <p><u>Intrinsic Support</u></p> <p>1:23-2:65; 4:39-51; 5:25-37; 6:15-26; 6:40-47; Fig. 3; Figs 4A-F; Application, 918,119, Original Drawings; August 27, 1997; Application, 918,119, Request for Patent Drawing Revision, December 16, 1998, United Kingdom Application, 9804417.5, Office Action, May 21, 1998; United Kingdom Application, 9804417.5, Response, March 4, 1999</p>	<p>Indefinite;</p> <p>or</p> <p>the first metal layer is about 1 to 4 μm greater than the width of the second metal layer measured from a level defined by the top of the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>Figs. 3-4; 1:20-2:65; 4:23-59; 5:21-38; 5:57-6:7; 6:27-48; App 08/918119, 11/17/98 Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
				09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance, page 2; App 08/918462, 4/26/99 Office Action, pages, 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462, 4/13/00 Response, pages 4- 8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9 10; App 09/983629, 8/8/01 Notice of Allowance, page 2

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
two side portions of the first metal layer having no second layer thereon	C	<p>the side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer</p> <p><u>Intrinsic Support</u></p> <p>2:5-26; 2:49-60; 3:21-29; 4:40-63; 5:21-38; 6:7-15; 6:27-49; 7:24-28; 7:47-52; Figs. 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment.</p>	Plain meaning	<p>the two side portions on the top surface of the first metal layer not covered by the second layer</p> <p><u>Intrinsic Support</u></p> <p>Figs. 3-4; 1:20-2:65; 4:23-59; 5:21-38; 5:57-6:7; 6:27-48 App 08/918119, 11/17/98 Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
				09/983629, 1/14/03 Notice of Allowance; page 2; App 08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462, 4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9-10; App 09/983629, 8/8/01 Notice of Allowance, page 2

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F
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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
two side portions of the first metal layer having no second layer disposed thereon	C A	<p>the side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer</p> <p><u>Intrinsic Support</u> 2:5-26; 2:49-60; 3:21-29; 4:40-63; 5:21-38; 6:7-15; 6:27-49; 7:24-28; 7:47-52; Figs. 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment.</p>	Plain meaning	<p>The two side portions on the top surface of the first metal layer not covered by the second layer</p> <p><u>Intrinsic Support</u> See above</p>

EXHIBIT G

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT G
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Disputed Constructions

Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
transistor	C	<p>A three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.</p> <p><u>Intrinsic Support</u></p> <p>1:20-40; 1:61-64; 2:64-68; 3:39-4:14; 5:56-58; Abstract.</p>	<p>A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate</p> <p>[The citations to the patent specification are to the column and line numbers in the grand-parent patent U.S. Patent No. 5,905,274.]</p> <p><u>Intrinsic Support</u></p> <p>1:15-15; 4:26-31; Fig. 2; Fig. 3</p>	<p>Plain meaning or A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate</p> <p><u>Intrinsic Support</u></p> <p>4:40-49; 4:57-62; 7:5-11</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
substrate	C	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support <u>Intrinsic Support</u> 2:65-3:5; 3:59-4:10; 5:59-64; Figs 1-4; Abstract.	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support	Plain meaning
forming a second metal layer on the first metal layer	L C	sequentially depositing the second metal layer above and in contact with the first metal layer <u>Intrinsic Support</u> 1:37-44; 2:65-3:37; 3:44-4:15; 4:44-56; 5:3-9; 5:39-55; 5:59-6:5; 7:47-67; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 4; App 09/243,556, 8/3/2001, Amendment; USP 6,340,610, Claims 1, 4.	The second metal layer is formed in direct contact with the first metal layer <u>Intrinsic Support</u> 3:49-51; Abstract; Fig. 3; Figs. 4A-F	forming a second metal layer above, supported by, and in contact with the first metal layer <u>Intrinsic Support</u> Fig. 4; 5:59-6:5

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
depositing a second metal layer on the first metal layer	L C	<p>sequentially depositing the second metal layer above and in contact with the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>1:37-44; 2:65-3:37; 3:44-4:15; 4:44-56; 5:3-9; 5:39-55; 5:59-6:5; 7:47-67; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 4; App 09/243,556, 8/3/2001, Amendment; USP 6,340,610, Claims 1, 4.</p>	<p>The second metal layer is deposited in direct contact with the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>3:49-51; Abstract; Fig. 3; Figs. 4A-F</p>	<p>Precipitating a second metal layer above, supported by, and in contact with the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Fig. 4; 5:59-6:5</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
a double layered metal gate	C A	<p>a patterned structure of an electrically conductive material that includes two sequentially deposited metal layers and includes a portion that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>1:20-56; 1:37-60; 3:4-36; 3:39-4:14; 4:40-52; 4:57-5:24; 5:39-55; 5:59-6:25; 6:33-65; 7:23-67; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 4; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance; USP 6,548,829, Claim 1.</p>	<p>a double-layered metal gate is a gate having only two metal layers</p> <p><u>Intrinsic Support</u></p> <p>1:17-23; 3:27-29; 4:32-34; 5:21-25; 6:27-29; Fig. 2; Fig. 3; Figs. 4A-F; Application 08/918,119, Response, November 17, 1998</p>	<p>a gate electrode having a two-layered step structure</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3-4; 1:29-3:14; 3:44-4:9; 4:41-5:9; 5:38-55; 6:44-47; 6:58-62</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
gate	L	<p>patterned electrically conductive material that includes a portion that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>1:20-56; 1:37-60; 3:4-36; 3:39-4:14; 4:40-52; 4:57-5:24; 5:39-55; 5:59-6:25; 6:33-65; 7:23-67; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 4; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance; USP 6,548,829, Claim 1.</p>	<p>a region of a transistor</p> <p><u>Intrinsic Support</u></p> <p>4:26-31; Fig. 2; Fig. 3</p>	<p>same as gate electrode; a patterned, electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.</p> <p><u>Intrinsic Support</u></p> <p>E.g., 4:41-5:20</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm	L C A	<p>the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more than 1 μm and less than 4 μm greater than the width of the second metal layer</p> <p><u>Intrinsic Support</u></p> <p>2:1-39; 3:59-4:15; 4:50-5:2; 5:38-55; 6:5-13; 6:18-65; 7:40-43; 7:62-67; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 2, 4, 5; App 09/243,556, 9/6/2000, Office Action; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance; USP</p>	<p>The top surface of the first metal layer has a width that is about 1 to 4 μm wider than a width of the top surface of the second metal layer to form a double step. A double step is a structure where not all of the top surface of the first metal layer is covered by the second metal layer.</p> <p><u>Intrinsic Support</u></p> <p>1:23-2:65; 4:39-51; 5:25-37; 6:15-26; 6:40-47; Fig. 3; Figs 4A-F; Application, 918,119, Original Drawings; August 27, 1997; Application, 918,119, Request for Patent Drawing Revision, December 16, 1998, United Kingdom Application, 9804417.5, Office Action, May 21, 1998; United Kingdom Application, 9804417.5, Response, March 4, 1999</p>	<p>Indefinite;</p> <p>or</p> <p>the width of the first metal layer is about 1 to 4 μm greater than the width of the second metal layer when measured from a level defined by the top of the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Indefinite: Figs. 3-4; 2:29-3:14; 4:40-5:9; 5:38-55; 6:14-25; 6:45-54 App 08/918119, 11/17/98 Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
		6,340,610, Claim 1; USP 6,548,829, Claims 1 and 6.		Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance, page 2; App 08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462, 4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9-10; App 09/983629, 8/8/01 Notice of Allowance, page 2

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
first etching layer	L	the first metal layer <u>Intrinsic Support</u> Claims 1-22; See Specification Generally.	Indefinite	Indefinite
waking	L	making <u>Intrinsic Support</u> Claims 1-22; See Specification Generally; App 10/377,732, 3/4/2003, Application as filed; App 10/377,732, 5/27/2004, Terminal Disclaimer Transmittal.	Indefinite	Non-sensical; indefinite

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
forming a single photoresist having a predetermined width on the second metal layer	C	<p>forming a pattern of single photosensitive material that has a specified width on the second metal layer</p> <p><u>Intrinsic Support</u></p> <p>1:40-60; 2:1-29; 2:65-36; 3:44-51; 3:66-4:9; 4:50-56; 5:58-6:44; 7:23-67; Figs. 1-4; Abstract; App 09/243,556, 9/6/2000, Office Action; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; USP 6,340,610 Claims 1, 2.</p>	<p>The photoresist is deposited in direct contact with the second metal layer</p> <p><u>Intrinsic Support</u></p> <p>3:41-58; 6:15-18; Figs. 4A-F</p>	Plain meaning
photoresist	C	<p>pattern of a photosensitive material</p> <p><u>Intrinsic Support</u></p> <p>1:40-60; 2:1-29; 2:65-36; 3:44-51; 3:66-4:9; 4:50-56; 5:58-6:44; 7:23-67; Figs. 1-4; Abstract.</p>	<p>An etching mask</p> <p><u>Intrinsic Support</u></p> <p>3:41-58; 6:15-18; Figs. 4A-F</p>	Plain meaning

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
simultaneously in a single etching step using the single photoresist as a mask	L	<p>during a single etching process with a common mask</p> <p><u>Intrinsic Support</u></p> <p>1:40-60; 2:1-29; 2:65-36; 3:44-51; 3:66-4:9; 4:50-56; 5:58-6:44; 7:23-67; Abstract; App 09/243,556, 9/6/2000, Office Action; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; USP 6,340,610, Claims 1, 2.</p>	<p>The first and second metal layers are simultaneously etched in a single step using the photoresist as a mask</p> <p><u>Intrinsic Support</u></p> <p>5:55-62; 7:15-30</p>	<p>construe term:</p> <p>"patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask"</p> <p>as</p> <p>forming the patterned first and second metal layers in one chemical etching step using one photoresist mask</p> <p><u>Intrinsic Support</u></p> <p>E.g., Fig. 4; 5:39-43; 6:6-12</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
simultaneously patterning/patterning . . . simultaneously	A	<p>removing part of the first and second metal layers during a single etching process</p> <p><u>Intrinsic Support:</u></p> <p>Abstract; 1:40-60; 2:1-29; 2:65-36; 3:44-51; 3:66-4:9; 4:50-56; 5:58-6:44; 7:23-67; Figs. 1, 4; USP 6,340,610, Claims 1, 2; App 09/243,556, 9/6/2000 Office Action; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001 Amendment.</p>	Plain meaning	<p>Forming the patterned first and second metal layers at the same time in one chemical etching step</p> <p><u>Intrinsic Support</u></p> <p>E.g., Fig. 4; 5:39-43; 6:6-12; App 08/918119, 11/17/98 Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance, page 2; App</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
				08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462, 4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages, 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9 10; App 09/983629, 8/8/01 Notice of Allowance, page 2

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
the first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4 μm	L C A	the first and second metal layers are etched such that the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more than 1 μm and less than 4 μm greater than the width of the second metal layer <u>Intrinsic Support</u> 2:1-39; 3:59-4:15; 4:50-5:2; 5:38-55; 6:5-13; 6:18-65; 7:40-43; 7:62-67; Figs. 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274 Claims 1, 2, 4, 5; App 09/243,556, 9/6/2000, Office Action; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App	The first metal layer being etched so that a top surface of the first metal layer has a width that is about 1 to 4 μm wider than a width of the top surface of the second metal layer to form a double step. A double step is a structure where not all of the top surface of the first metal layer is covered by the second metal layer. <u>Intrinsic Support</u> 1:23-2:65; 4:39-51; 5:25-37; 6:15-26; 6:40-47; Fig. 3; Figs 4A-F; Application, 918,119, Original Drawings; August 27, 1997; Application, 918,119, Request for Patent Drawing Revision, December 16, 1998, United Kingdom Application, 9804417.5, Office Action, May 21, 1998; United Kingdom Application, 9804417.5, Response, March 4, 1999	indefinite; or the first metal layers being etched so that the width of the first metal layer is about 1 to 4 μm greater than the width of the second metal layer when measured from a level defined by the top of the first metal layer <u>Intrinsic Support</u> E.g., Indefinite: Figs. 3-4; 2:29-3:14; 4:40-5:9; 5:38-55; 6:14-25; 6:45-54 App 08/918119, 11/17/98 Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
		09/243,556, 9/10/2001, Notice of Allowance; USP 6,340,610, Claim 1; USP 6,548,829, Claims 1 and 6.		Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance, page 2; App 08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462, 4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages, 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9 10; App 09/983629, 3/8/01

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
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a first and a second side portion being exposed from the second metal layer	C	<p>first and second side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer</p> <p><u>Intrinsic Support</u></p> <p>1:34-60; 2:65-3:14; 3:39-47; 3:52-57; 5:38-55; 6:55-65; 7:62-67; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 2, 4, 5; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance.</p>	Plain meaning	<p>A first side portion and a second side portion on the top surface of the first metal layer not covered by the second layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Indefinite: Figs. 3-4; 4:40-5:9; 5:38-55; 6:45-54; 6:58-62 App 08/918119, 11/17/98 Response, pages 3-4,; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action,</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
				pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance, page 2; App 08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462, 4/13/00 Response, pages 4- 8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4- 10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9-10; App 09/983629, 8/8/01 Notice of Allowance, page 2

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
two side portions of the first metal layer having no second metal layer deposited thereon	C A	<p>the side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer</p> <p><u>Intrinsic Support</u></p> <p>1:34-60; 2:65-3:14; 3:39-47; 3:52-57; 5:38-55; 6:55-65; 7:62-67; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 2, 4, 5; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance</p>	Plan meaning	<p>The two portions on the top surface of the first metal layer not covered by the second metal layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Indefinite: Figs. 3-4; 4:40-5:9; 5:38-55; 6:45-54; 6:58-62 App 08/918119, 11/17/98 Response, pages 3-4,; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
				11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance, page 2; App 08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462, 4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9-10; App 09/983629, 8/8/01 Notice of Allowance, page 2

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
the first metal layer including aluminum	C	<p>the first metal layer containing aluminum and possibly other materials</p> <p><u>Intrinsic Support</u></p> <p>1:20-28; 1:34-44; 1:56-60; 2:1-5; 3:39-44; 4:50-56; 5:59-6:5; 7:62-67; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 4; App 09/243,556, 3/11/1999, Preliminary Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment.</p>	<p>A first metal layer that includes pure aluminum</p> <p><u>Intrinsic Support</u></p> <p>4:34-36; 5:41-42</p>	Plain meaning

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Disputed Constructions

Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
transistor	C	<p>A three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.</p> <p><u>Intrinsic Support</u></p> <p>1:20-40; 1:61-64; 2:64-68; 3:39-4:14; 5:56-58; Abstract.</p>	<p>A three-terminal semiconductor device in which the current flow through one pair of, electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate</p> <p><u>Intrinsic Support</u></p> <p>1:15-16; 4:26-31; Fig. 2; Fig. 3</p>	<p>Plain meaning</p> <p>or</p> <p>A three-terminal semiconductor device in which the current flow through one pair of, electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate</p> <p><u>Intrinsic Support</u></p> <p>E.g., 4:41-50; 4:58-63; 7:5-11</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
substrate	C	<p>the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support</p> <p><u>Intrinsic Support:</u></p> <p>2:64-3:3; 3:59-4:8; 5:59-64; Figs 1-4; Abstract.</p>	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support	<p>Plain meaning;</p> <p>or</p> <p>The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
a double layered metal gate	C A	<p>a patterned structure of an electrically conductive material that includes two sequentially deposited metal layers and includes a portion that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>1:21-56; 1:38-60; 3:4-34; 3:39-4:13; 4:41-53; 4:58-5:25; 5:39-55; 5:59-6:25; 6:33-65; 7:24-8:26; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 4; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance; USP 6,548,829, Claim 1.</p>	<p>a gate having only two metal layers</p> <p><u>Intrinsic Support</u></p> <p>1:17-23; 3:27-29; 4:32-34; 5:21-25; 6:27-29; Fig. 2; Fig. 3; Figs. 4A-F; Application, 08/918,119, Response, November 17, 1998</p>	<p>A gate electrode having a two-layered step structure</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3-4; 1:29-3:14; 3:44-4:9; 4:41-5:9; 5:38-55; 6:44-47; 6:58-62</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
gate	L	<p>patterned electrically conductive material that includes a portion that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>1:21-56; 1:38-60; 3:3-35; 3:39-4:13; 4:41-53; 4:58-5:25; 5:39-55; 5:59-6:25; 6:33-65; 7:24-8:26; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 4; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance; USP 6,548,829, Claim 1.</p>	<p>a region of a transistor</p> <p><u>Intrinsic Support</u></p> <p>4:26-31; Fig. 2; Fig. 3</p>	<p>same as gate electrode; a patterned electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode</p> <p><u>Intrinsic Support</u></p> <p>E.g., 3:44-50; 4:41-5:21</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
having a first metal layer and a second metal layer thereon	L C	<p>sequentially depositing the second metal layer above and in contact with the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>1:38-44; 2:64-3:37; 3:44-4:13; 4:44-57; 5:4-10; 5:39-55; 5:59-6:5; 8:6-26; Figs 1-4; Abstract; App 8/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 4; App 09/243,556, 8/3/2001, Amendment; USP 6,340,610, Claims 1, 4.</p>	<p>the second metal layer is in contact with the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>3:49-51; Abstract; Fig. 3; Figs. 4A-F</p>	<p>The double layered metal gate having a first metal layer and a second metal layer formed on the top surface of the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3-4; 5:59-6:5</p>
a total width of the first metal layer being greater than a total width of the second metal layer by about 1 to 4 μm	L C A	<p>the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more than 1 μm and less than 4 μm greater than the width of the second metal layer</p>	<p>The top surface of the first metal layer has a width that is about 1 to 4 μm wider than a width of the top surface of the second metal layer to form a double step. A double step is a gate where not all of the top surface of the first metal layer is covered by the second metal layer.</p>	<p>Indefinite;</p> <p>or</p> <p>The width of the first metal layer is about 1 to 4 μm greater than the width of the second metal measured from a level defined by the top of the first metal layer</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
		<u>Intrinsic Support</u> 2:1-38; 3:58-4:13; 4:51-5:3; 5:39-55; 6:6-13; 6:18-65; 7:41-8:2; 8:21-26; Figs. 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 2, 4, 5; App 09/243,556, 9/6/2000, Office Action; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance; USP 6,340,610, Claim 1; USP 6,548,829, Claims 1 and 6.	<u>Intrinsic Support</u> 1:23-2:65; 4:39-51; 5:25-37; 6:15-26; 6:40-47; Fig. 3; Figs 4A-F; Application, 918,119, Original Drawings; August 27, 1997; Application, 918,119, Request for Patent Drawing Revision, December 16, 1998, United Kingdom Application, 9804417.5, Office Action, May 21, 1998; United Kingdom Application, 9804417.5, Response, March 4, 1999	<u>Intrinsic Support</u> Indefinite: Figs. 3-4; 2:29-3:14; 4:40- 5:9; 5:38-55; 6:14-25; 6:45-54; App 08/918119, 11/17/98 Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
				<p>Notice of Allowance, page 2; App 08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6 ; App 08/918462, 4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9 10; App 09/983629, 8/8/01 Notice of Allowance, page 2</p>
a first and second side portion being exposed from the second metal layer	C A	first and second side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer	Plain meaning	The two side portions on the top surface of the first metal layer not covered by the second metal layer

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
		<u>Intrinsic Support</u> 1:35-60; 2:64-3:13; 3:39-46; 3:51-57; 5:39-55; 6:55-65; 8:21-26-; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 2, 4, 5; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance.		<u>Intrinsic Support</u> E.g., Figs. 3-4; 4:40-5:9; 5:38-55; 6:45-55; 6:58-63; App 08/918119, 11/17/98 Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages, 2-5; App 09/243556, 8/3/91 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance, page 2; App 08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
				1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462, 4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9-10; App 09/983629, 8/8/01 Notice of Allowance., page 2
side portion of the first metal layer	A	<p>side surface of the first metal layer exposed to the subsequently deposited gate insulating layer</p> <p><u>Intrinsic Support</u></p> <p>1:35-60; 2:64-3:13; 3:39-50; 3:51-57; 5:39-55; 6:55-65;</p>	Plain meaning	<p><i>Construed with "each" in front:</i></p> <p>Each of the first and second side portions on the top surface of the first metal layer not covered by the second metal layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3-4; 4:40-5:9; 5:38-55; 6:45-55 6:58-62;</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
		8:21-26; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 2, 4, 5; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance.		App 08/918119, 11/17/98 Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance, page 2; App 08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action,

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
				pages 3-6; App 08/918462, 4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9-10; App 09/983629, 8/8/01 Notice of Allowance, page 2

EXHIBIT I

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT I
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Claim Terms	Des.	Agreed Constructions
UV sealant	C	sealant material that is at least partially curable by UV light
forming a main UV sealant	L	The combination of the construction for “forming a main sealant” with the agreed construction of “UV sealant”
auxiliary UV sealant	C A	The combination of the construction for “auxiliary sealant” with the agreed construction of “UV sealant”
main UV sealant	C A	The combination of the construction for “main sealant” with the agreed construction of “UV sealant”

Disputed Constructions

Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
preparing a lower substrate and an upper substrate	C	making the substrates ready for depositing sealant and liquid crystal material prior to attachment <u>Intrinsic Support</u> 4:30-67; Fig. 3A.	Indefinite	Indefinite <u>Intrinsic Support</u> E.g., Figs. 3, 4, 5, & 6; 4:23-67; 6:40-67; 7:27-58; 7:64-34
forming a main sealant	L	depositing sealant material that encloses the display region <u>Intrinsic Support</u> 2:36-40; 3:20-25, 5:5-7; Figs. 2B, 3B, 4A, and 5A.	forming sealant material necessary for confining liquid crystal from leaking out from between the substrates <u>Intrinsic Support</u> Abstract; 3:20-24; 3:35-41; 3:55-4:11; 5:3-30; 6:34-39;	forming a segment of sealant that encloses the liquid crystal in the LCD panel <u>Intrinsic Support</u> E.g., Figs. 3, 4, 5, & 6; 3:9-40; 5:1-64; 6:40-67 App 10/184118, 12/1/03 OA,

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
			7:11-16; 7:63-8:2; Figs. 1A-1D, 2A-2C, 3A-3D, 4A-4D, 5A-5B, 6	pages 2-7; App 10/184118, 2/4/04 Amendment in Response to Non-Final Office Action, pages 7-9; App 10/184118, 04/26/2004, pages 2-7; App 10/184118, 7/15/2004 Reply Under 37 C.F.R. Section 1.111, pages 2-6 App 10/184118, 11/18/2004 OA, pages 2-8; App 10/184118, 02/16/2005 Response after Office Action, pages 2-7; App 10/184118, 04/18/2005 Response as Submission under 37 C.F.R. 1.114, pages 6-11; App 10/184118, 06/15/2005 Office Action, pages 2-4; App 10/184118, 09/15/2005 Response to non-final Office Action, pages 6-7; App 10/184118, 12/01/2005 Office Action, pages 2-4; App 10/184118, 03/01/2006 Response to Final Office Action, pages 7; App 10/184118, 06/19/2006 Office Action, pages 2-8; App 10/184118, 09/15/2006 Response to Non-final Office Action, page 5; App 10/184118,

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
				10/11/2006 Notice of Allowability, page 2.
main sealant	C A	sealant material that encloses the display region <u>Intrinsic Support</u> 2:36-40; 3:20-25, 5:5-20; 7:63-8:2; Figs. 2B, 3B, 4A, and 5A.	sealant material necessary for confining liquid crystal from leaking out from between the substrates <u>Intrinsic Support</u> Abstract; 3:20-24; 3:35-41; 3:55-4:11; 5:3-30; 6:34-39; 7:11-16; 7:63-8:2; Figs. 1A-1D, 2A-2C, 3A-3D, 4A-4D, 5A-5B, 6	A segment of sealant for enclosing the liquid crystal in the LCD panel <u>Intrinsic Support</u> See above
auxiliary sealant	C A	sealant deposited in an area outside of the main sealant <u>Intrinsic Support</u> 5:7-20; 7:63-8:2; Figs. 3B, 4A, and 5A.	sealant material that is not necessary for confining liquid crystal from leaking out from between the substrates <u>Intrinsic Support</u> Abstract; 1:20-23; 3:20-24; 3:35-41; 3:55-4:11; 5:3-20; 6:34-39; 7:11-16; 7:63-8:2; Figs. 1A-1D, 2A-2C, 3A-3D, 4A-4D, 5A-5B, 6	A segment of sealant for that extends from the main sealant and is outside the enclosure of the main sealant <u>Intrinsic Support</u> E.g., Fig. 4, 5, & 6; 3:9-40; 5:1-64; 6:40-67

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
a dummy region	L A	<p>an area outside of the main sealant</p> <p><u>Intrinsic Support</u></p> <p>5:7-20; 7:63-8:2; Figs. 3B, 4A, and 5A.</p>	<p>an area outside the boundary of the main sealant</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:20-23; 2:5-55; 3:9-40; 3:55-4:11; 5:3-20; 5:27-51; 6:34-39; 7:63-8:2; 8:14-17; Figs. 1A-1D, 2A-2C, 3A-3D, 4A-4D, 5A-5B, 6; App. 10/184,118, 11/18/04 Office Action, page 2-3; 2/16/05 Amendment at page 2</p>	<p>An area outside the , enclosure of the main sealant</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2, 3, 4, 5, & 6; 2:47-54; 3:9-40; 5:1-64; 6:40-67</p>
connects to the main sealant	L	<p>joined to the main sealant</p> <p><u>Intrinsic Support</u></p> <p>2:41-55; 5:7-20; 7:63-8:2; Figs. 3B, 4A, and 5A; App 10/184,118, 7/16/04, Response, page 2; App 10/184,118, 2/16/05 Response, pages 2-3; App 10/184,118, 4/18/05 Response, pages 6-7; App 10/184,118, 11/27/06 Response, page 2.</p>	<p>physically attached to the main sealant</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:20-23; 2:5-55; 3:9-40; 3:55-4:11; 5:3-20; 5:27-51; 6:34-39; 7:63-8:2; 8:14-17; Figs. 1A-1D, 2A-2C, 3A-3D, 4A-4D, 5A-5B, 6; App. 10/184,118, 11/18/04 Office Action, page 2-3; 2/16/05 Amendment at page 2</p>	<p>Physically attached to the main sealant</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, 5, & 6; 5:1-64; 6:40-67</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
wherein the auxiliary UV sealant is formed in a dummy region and extends outside from the main UV sealant	L C A	<p>wherein the auxiliary UV sealant is deposited in an area that is outside of the main UV sealant and is joined to the main UV sealant</p> <p><u>Intrinsic Support</u></p> <p>2:41-55; 5:7-20; 7:63-8:2; Figs. 3B, 4A, and 5A; App 10/184,118, 7/16/04, Response, page 2; App 10/184,118, 2/16/05 Response, pages 2-3; App 10/184,118, 4/18/05 Response, pages 6-7 App 10/184,118, 11/27/06 Response, page 2.</p>	<p>wherein the auxiliary UV sealant is formed in an area outside the boundary of the main UV sealant beginning from the main UV sealant and moving outward</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:20-23; 2:5-55; 3:9-40; 3:55-4:11; 5:3-20; 5:27-51; 6:34-39; 7:63-8:2; 8:14-17; Figs. 1A-1D, 2A-2C, 3A-3D, 4A-4D, 5A-5B, 6; App. 10/184,118, 3/1/06 Response, pages 5, 7</p>	<p>Wherein the auxiliary UV sealant is formed in an area outside the enclosure of the main UV sealant</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, 5, & 6; 5:1-6:9; 6:40-67</p>
wherein the auxiliary sealant and the main sealant are contiguous	L C A	<p>wherein the auxiliary and main sealants are deposited in a continuous process</p> <p><u>Intrinsic Support</u></p> <p>2:41-55; 5:7-20; 7:63-8:2; Figs. 3B, 4A, and 5A; App 10/184,118, 7/16/04, Response, page 2; App 10/184,118, 2/16/05 Response, pages 2-3; App</p>	<p>wherein the auxiliary sealant touches but does not overlap the main sealant</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:20-23; 2:5-55; 3:9-40; 3:55-4:11; 5:3-20; 5:27-51; 6:34-39; 7:63-8:2; 8:14-17; Figs. 1A-1D, 2A-2C, 3A-3D, 4A-4D, 5A-5B, 6; App. 10/184,118, 6/19/06</p>	<p>Wherein the auxiliary sealant and the main sealant are physically connected to each other</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, 5, & 6; 5:1-64; 6:40-67 App 10/184118, 12/1/03 OA, pages 2-7; App 10/184118, 2/4/04 Amendment in Response to Non-Final Office Action,</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
		10/184,118, 4/18/05 Response, pages 6-7; App 10/184,118, 11/27/06 Response, page 2.	Office Action, page 3, 4; 9/15/06 Amendment, page 2, 5	pages 7-9; App 10/184118, 04/26/2004, pages 2-7; App 10/184118, 7/15/2004 Reply Under 37 C.F.R. Section 1.111, pages 2-6 App 10/184118, 11/18/2004 OA, pages 2-8; App 10/184118, 02/16/2005 Response after Office Action, pages 2-7; App 10/184118, 04/18/2005 Response as Submission under 37 C.F.R. 1.114, pages 6-11; App 10/184118, 06/15/2005 Office Action, pages 2-4; App 10/184118, 09/15/2005 Response to non-final Office Action, pages 6-7; App 10/184118, 12/01/2005 Office Action, pages 2-4; App 10/184118, 03/01/2006 Response to Final Office Action, pages 7; App 10/184118, 06/19/2006 Office Action, pages 2-8; App 10/184118, 09/15/2006 Response to Non-final Office Action, page 5; App 10/184118, 10/11/2006 Notice of Allowability, page 2

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT I
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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
wherein the auxiliary UV sealant contacts the main UV sealant	C A	<p>wherein the auxiliary UV sealant touches the main UV sealant</p> <p><u>Intrinsic Support</u></p> <p>2:41-55; 5:7-20; 7:63-8:2; Figs. 3B, 4A, and 5A; App 10/184,118, 7/16/04, Response, page 2; App 10/184,118, 2/16/05 Response, pages 2-3; App 10/184,118, 4/18/05 Response, pages 6-7; App 10/184,118, 11/27/06 Response, page 2.</p>	<p>wherein the auxiliary UV sealant touches the main UV sealant</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:20-23; 2:5-55; 3:9-40; 3:55-4:11; 5:3-20; 5:27-51; 6:34-39; 7:63-8:2; 8:14-17; Figs. 1A-1D, 2A-2C, 3A-3D, 4A-4D, 5A-5B, 6; App. 10/184,118, 6/19/06 Office Action, page 3, 4; 9/15/06 Amendment, page 4, 5</p>	<p>wherein the auxiliary sealant and the main sealant are physically connected together</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, 5, & 6; 5:1-6:9; 6:40-67</p>
applying a liquid crystal on one of the lower and upper substrates	L C A	<p>depositing the liquid crystal onto either one of the substrates</p> <p><u>Intrinsic Support</u></p> <p>5:65 - 6:9; Fig. 3B.</p>	<p>plain meaning</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:31-55; 2:5-15; 2:34-40; 3:25-34; 5:27-5:51; Figs. 1A-1D; 3A-3D</p>	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, 5, & 6; 5:65-6:9; 6:40-67 App 10/184118, 12/1/03 OA, pages 2-7; App 10/184118, 2/4/04 Amendment in Response to Non-Final Office Action, pages 7-9; App 10/184118, 04/26/2004, pages 2-7; App</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
				<p>10/184118, 7/15/2004 Reply Under 37 C.F.R. Section 1.111, pages 2-6 App 10/184118, 11/18/2004 OA, pages 2-8; App 10/184118, 02/16/2005 Response after Office Action, pages 2-7; App 10/184118, 04/18/2005 Response as Submission under 37 C.F.R. 1.114, pages 6-11; App 10/184118, 06/15/2005 Office Action, pages 2-4; App 10/184118, 09/15/2005 Response to non-final Office Action, pages 6-7; App 10/184118, 12/01/2005 Office Action, pages 2-4; App 10/184118, 03/01/2006 Response to Final Office Action, pages 7; App 10/184118, 06/19/2006 Office Action, pages 2-8; App 10/184118, 09/15/2006 Response to Non-final Office Action, page 5; App 10/184118, 10/11/2006 Notice of Allowability, page 2</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
attaching the lower and upper substrates	A	<p>pressing the lower and upper substrates together</p> <p><u>Intrinsic Support</u></p> <p>6:4-6; Figs. 1C and 2C.</p>	<p>putting the lower and upper substrates together as one single piece</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:27-28; 3:25-34; 5:65-6:15; Figs. 1A-1D; 3A 3D</p>	<p>Putting the lower and upper substrates together as one single piece</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, 5, & 6; 5:65-6:9; 6:40-67</p>

EXHIBIT J

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT J
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Claim Terms	Des.	Agreed Constructions
color filter	L	A filter that modifies light from a source so as to allow one or more selected colors to pass through to the viewer side of the display. A color filter is formed on the color filter substrate.
color filter substrate	A	the structure on which the color filter is formed that faces the TFT substrate
active element	A	an element that controls voltage or current, typically one or more transistors located at each pixel location

Disputed Constructions

Claim Terms	Des.	AUO Construction	LGD Construction
common electrode	L	<p>a conductor, typically made of a transparent material, on the color filter substrate that receives a reference voltage relative to which the pixel electrode voltages can be measured</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:57-60, Figs. 1 and 2; 2:1-12; 2:25-3:29, esp. 2:29-42, and Figs. 3 and 4; 3:35-38, and Fig. 2; 4:65-5:44, esp. 4:67-5:6, and Fig 8; 6:26-43, 6:47-51, and Figs. 6-11, esp. element 30; 6:52-7:32, esp. 7:8-19; 8:24-25; claims 1, 3, 6, and 7.</p>	<p>a conductor, typically made of a transparent material, on the color filter substrate that receives a reference voltage relative to the pixel electrode voltages</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:57-2:04; 2:25-42; 2:43-3:65; 5:07-10; 7:09-14; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11.</p>

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Claim Terms	Des.	AUO Construction	LGD Construction
pillars formed higher than other portions of the color filter	L	<p>the pillars are formed higher than the highest portions of the color filter.</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 4:65-5:6, and Fig. 8; 5:57-6:5; 6:26-43, 6:47-51, and Figs. 6-11, esp. elements 78 and 32; 7:4-31, and Fig. 8; 8:20-23; claims 1-5, 7, 9 and 10; March 5, 1997 Office Action, esp. at 2-3; July 7, 1997 Response, esp. at 6-7.</p>	<p>patterned structures of the color filter that protrude toward the pixel array beyond the height of non-pillar portions of the color filter substrate to act as a spacer</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:13-19; 3:66-4:21; 4:21-30; 4:31-49; 4:51-64; 4:65-5:06; 5:07-10; 5:57-6:05; 7:09-14; 7:32-43; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11; JP H08-262484 at paragraphs [0017]-[0032]; App 08/615,012, 7/7/1997 Amendment, pages 2-7.</p>
objects formed on the array substrate	L	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 4:65-5:6, and Fig. 8; 5:57-6:5; 6:26-43, 6:47-51, and Figs. 6-11; 7:4-31, and Fig. 8; 8:28-34; claims 1, 3, 6 and 7. March 5, 1997 Office Action, esp. at 2-3; July 7, 1997 Response, esp. at 6-7.</p>	<p>structures having one or more patterned layers in the pixel array</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:13-19; 3:66-4:21; 4:21-30; 4:31-49; 4:51-64; 4:65-5:06; 5:07-10; 5:57-6:05; 7:09-14; 7:32-43; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11; JP H08-262484 at paragraphs [0017]-[0032]; App 08/615,012, 7/7/1997 Amendment, pages 2-7.</p>

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Claim Terms	Des.	AUO Construction	LGD Construction
the pillars are covered with the common electrode	L	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 4:65-5:6, and Fig. 8; 6:26-43, 6:47-51, and Figs. 6-11, esp. elements 78 and 30; 7:4-13, and Fig. 8; 8:24-25; 8:28-34; claims 1, 3 and 7; March 5, 1997 Office Action, esp. at 2-3; July 7, 1997 Response, esp. at 6-7.</p>	<p>the common electrode is formed to cover the protruded surface of the pillars</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:57-2:04; 2:13-19; 2:25-42; 2:43-3:65; 3:66-4:21; 4:21-30; 4:31-49; 4:51-64; 4:65-5:06; 5:07-10; 5:57-6:05; 7:09-14; 7:32-43; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11; JP H08-262484 at paragraphs [0017]-[0032]; App 08/615,012, 7/7/1997 Amendment, pages 2-7.</p>
pillars being formed higher than other portions of the facing substrate	L	<p>the pillars are formed higher than the highest portions of the color filter substrate.</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 4:65-5:6, and Fig. 8; 5:57-6:5; 6:26-43, 6:47-51, and Figs. 6-11, esp. elements 78 and 32; 7:4-31, and Fig. 8; 8:20-23; claims 1-5, 7, 9 and 10; March 5, 1997 Office Action, esp. at 2-3; July 7, 1997 Response, esp. at 6-7.</p>	<p>patterned structures that protrude toward the pixel array beyond the height of non-pillar portions of the color filter substrate to act as a spacer</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:13-19; 3:66-4:21; 4:21-30; 4:31-49; 4:51-64; 4:65-5:06; 5:07-10; 5:57-6:05; 7:09-14; 7:32-43; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11; JP H08-262484 at paragraphs [0017]-[0032]; App 08/615,012, 7/7/1997 Amendment, pages 2-7.</p>

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Claim Terms	Des.	AUO Construction	LGD Construction
common electrode for all pixels covering at least some of the pillars	L	<p>Plain meaning:</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 4:65-5:6, and Fig. 8; 6:26-43, 6:47-51, and Figs. 6-11, esp. elements 78 and 30; 7:4-13, and Fig. 8; 8:24-25; 8:28-34; claims 1, 3 and 7; March 5, 1997 Office Action, esp. at 2-3; July 7, 1997 Response, esp. at 6-7.</p>	<p>the common electrode is formed on the protruded surface of at least some of the pillars</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:57-2:04; 2:25-42; 2:43-3:65; 4:31-49; 4:51-64; 4:65-5:06; 5:07-10; 5:57-6:05; 7:09-14; 7:32-43; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11; JP H08-262484 at paragraphs [0017]-[0032]; App 08/615,012, 7/7/1997 Amendment, pages 2-7.</p>
the common electrode being electrically connected to the storage capacitance line at the portions of the common electrode covering the pillars	L	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 4:65-5:44, and Fig. 8; 6:26-43, 6:47-51, and Figs. 6-11; 7:4-43, and Fig. 8; 8:24-25; 8:28-34; claims 1, 3 and 7; March 5, 1997 Office Action, esp. at 2-3; July 7, 1997 Response, esp. at 6-7.</p>	<p>the common electrode is electrically connected to the storage capacitance line in the pixel area where the pillars covered with the common electrode contact the objects on the array substrate</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:45-48; 1:57-2:04; 2:13-19; 2:25-42; 2:43-3:65; 4:31-49; 4:51-64; 4:65-5:06; 5:07-10; 5:57-6:05; 7:09-14; 7:32-43; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11; JP H08-262484 at paragraphs [0017]-[0032]; App 08/615,012, 7/7/1997 Amendment, pages 2-7.</p>

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Claim Terms	Des.	AUO Construction	LGD Construction
storage capacitance line for outputting the reference potential of the storage capacitance	L	<p>the storage capacitance line is connected to the capacitor(s), and therefore outputs the reference potential of the storage capacitance</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:45-48, and Figs. 1 and 2; 2:31-40, and Figs. 3 and 4; 4:65-5:44, and Fig. 8; 6:26-43, 6:47-51, and Figs. 6-11, esp. element 28; claims 3, 6, 7, and 9; March 5, 1997 Office Action, esp. at 2-3; July 7, 1997 Response, esp. at 6-7.</p>	<p>a pattern of electrically conductive material within the pixel area for providing a reference voltage to the storage capacitors</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:45-48; 1:57-2:04; 2:25-42; 2:43-3:65; 4:31-49; 4:65-5:06; 5:07-10; 7:09-14; 7:32-43; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11; JP H08-262484 at paragraphs [0017]-[0032]; App 08/615,012, 7/7/1997 Amendment, pages 2-7.</p>
storage capacitance line	A	<p>a line or wire of conductive material, typically metal, connected to one or more storage capacitors of the TFT array</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:45-48, and Figs. 1 and 2; 2:31-40, and Figs. 3-4; 4:67-5:44, esp. 5:14-18, and Fig. 8; 6:26-43, 6:47-51, and Figs. 6-11, esp. element 28; claims 3, 6, 7, and 9; March 5, 1997 Office Action, esp. at 2-3; July 7, 1997 Response, esp. at 6-7.</p>	<p>a pattern of electrically conductive material within the pixel area for providing a reference voltage to the storage capacitors</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:45-48; 1:57-2:04; 2:25-42; 2:43-3:65; 4:31-49; 4:65-5:06; 5:07-10; 7:09-14; 7:32-43; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11; JP H08-262484 at paragraphs [0017]-[0032]; App 08/615,012, 7/7/1997 Amendment, pages 2-7.</p>

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Claim Terms	Des.	AUO Construction	LGD Construction
pillars of a color filter	L	<p>pillars associated with and constructed on the color filter, for maintaining separation between the array substrate and the color filter substrate</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 4:65-5:6, and Fig. 8; 5:57-6:5; 6:26-43, 6:47-51, and Figs. 6-11, esp. element 78; 7:4-32, and Fig. 8; 8:20-23; claims 1-5, 7, 9, and 10.</p>	<p>patterned structures that protrude toward the pixel array, to act as a spacer, and are made of color filter material</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:13-19; 3:66-4:21; 4:21-30; 4:31-49; 4:51-64; 4:65-5:06; 5:07-10; 5:57-6:05; 7:09-14; 7:32-43; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11; JP H08-262484 at paragraphs [0017]-[0032]; App 08/615,012, 7/7/1997 Amendment, pages 2-7.</p>
injecting liquid crystal between the array substrate and the color filter substrate	L	<p>Introducing liquid crystal into the space between the array substrate and the color filter substrate</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:17-18, and Fig. 2; 6:26-43, 6:47 51, and Figs. 6-11; 7:51-8:39, esp. 8:35-39; claim 9; U.S. Patent No. 5,181,132 (Shindo et al.) in general, esp.: 2:9-18 and Fig. 2; 2:19-37 and Fig. 3; 10:39-49 and Fig. 10; 11:15-22 and Fig. 12; 13:27-32 and Fig. 16. U.S. Patent No. 5,338,240 (Kim) in general, esp.: 1:64-66 and Fig.1; 4:31-34 and Fig. 3.</p>	<p>providing liquid crystal through an injection hole between the sealed array and color filter substrates</p> <p><u>Intrinsic Support</u></p> <p>7:62-8:39</p>

EXHIBIT K

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT K
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Claim Terms	Des.	Agreed Constructions
connection pads	L	conductive patterns on the substrate that electrically connect the plurality of wiring to circuits located external to the substrate

Disputed Constructions

Claim Terms	Des.	AUO Construction	LGD Construction
a layer of an insulating substrate, having an area	L	<p>plain meaning</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:12-20, esp. 14-20; 1:32-46, esp. 39-44; 2:13-24, esp. 17-21; 3:11-28, esp. 11-14; 3:29-47, esp. 29-37; 4:33-41; 6:17-34, esp. 23-27, 30-34; claims 1, 9; Figures 1, 5a-5c, 11, 12a-12b; May 29, 2003 Office Action, esp. at 2. U.S. Patent No. 5,285,301 (Shirahashi et al.) 3:37-44, esp. 39-40.</p> <p>Included is the intrinsic support for the disputed term: "area".</p>	<p>material deposited and patterned on a substrate, such as glass, that covers part of the array substrate surface</p> <p><u>Intrinsic Support</u></p> <p>1:7-11; 1:21-2:63; 2:67- 3:6; 3:12-22; 3:26-28; 3:30-51; 3:60-4:23; 4:39-42; 4:55-5:26; 5:29-43; 5:46-6:6; 6:9-47; 6:59-67; 7:5-19; 7:24-27; 7:31-40; 7:50-62; Figs. 2-5, 8, 9, 10; App 10/068,500, 5/29/2003, Office Action, page 2-4.</p>

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Claim Terms	Des.	AUO Construction	LGD Construction
area	A	<p>a specified region</p> <p><u>Intrinsic Support</u></p> <p>1:61-67, esp. 63-66; 2:51-62, esp. 51-54; 3:11-28, esp. 18-19; 3:29-47, esp. 38-39; 5:29-42, esp. 29-33, 38-42; 5:43-53; 5:54-60, esp. 54-57; 5:61-6:6, esp. 5:61-6:1, 6:4-6; 6:35-47, esp. 35-40; claims 1, 9; Japanese Laid Open No. H10-90706, esp. at TR 0003, 0015, 0017, 0020, 0023, 0024, and Figure 5; May 29, 2003 Office Action, esp. at 2. U.S. Patent No. 5,285,301 (Shirahashi et al.) 11:11-14; 11:54-58.</p>	<p>Indefinite</p> <p>or</p> <p>(see above)</p>

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Claim Terms	Des.	AUO Construction	LGD Construction
a plurality of wiring arranged on the insulating substrate	L	<p>two or more conductive paths disposed on the insulating substrate</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:12-20, esp. 14-20; 1:28-30; 1:32-46, esp. 39-44; 2:13-24, esp. 17-21; 3:11-28, esp. 13-24; 3:29-47, esp. 32-47; 4:33-41, esp. 38-41; 5:29-42, esp. 29-33, 38-42; 6:17-34, esp. 23-27, 30-34; 6:35-47, esp. 35-40; claims 1, 2, 10; Figures 1, 3, 4, 5a-5c, 11, 12a-12b; Japanese Laid Open H10-90706, esp. ¶ 0009; Japanese Laid Open H10-240150, esp. ifif 0002, 0003, 0013 May 29, 2003 Office Action, esp. at 2. U.S. Patent No. 5,285,301 (Shirahashi et al.) 6:10-20.</p> <p>Included is the intrinsic support for the disputed term: "a layer of an insulating substrate, having an area".</p>	<p>portions of the layer that convey voltages or signals from the connection pads to the thin-film transistors in the pixel array</p> <p><u>Intrinsic Support</u></p> <p>1:8-2:63; 2:66-3:6; 3:14-15; 3:22-29; 3:31-35; 3:42-48; 3:60-4:23; 4:39-42; 4:52-5:28; 5:34-43; 5:55-6:16; 6:24-47; 6:55-7:40; 7:50-62; Abstract; Figs. 2-11; App 10/068,500, 5/29/2003, Office Action, page 2-4.</p>

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Claim Terms	Des.	AUO Construction	LGD Construction
dummy conductive patterns	L A	<p>a metal pattern that does not conduct signals or current used in the operation of the display</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:12-20, esp. 14-20; 1:32-46, esp. 39-44; 1:46-59, esp. 49-54; 2:13-24, esp. 17-21; 3:11-28, esp. 17-22; 3:29-47, esp. 35-41; 3:66-4:2; 5:29-42, esp. 29-33, 38-42; 5:43-53; 6:14-17; 6:37-38; 6:52-55; claims 1, 9; Figures 2-4, 5a-5c. May 29, 2003 Office Action, esp. at 2. U.S. Patent No. 6,163,356 (Song et al.) 7:31-63; 8:27-40; 8:41-67. U.S. Patent No. 5,285,301 (Shirahashi et al.) 6:10-18; 13:30-61, esp. 45-61; claims 3, 4; Figures 1, 14, 15.</p>	<p>portions of the layer that do not receive or convey voltages or signals</p> <p><u>Intrinsic Support</u></p> <p>1:32-67; 2:25-63; 3:3-19; 3:21-29; 3:33-38; 4:34-42; 4:52-55; 5:11-54; 5:64-66; 6:24-38; 6:52-67; 7:15-35; 7:50-63; Abstract; Fig. 2-4.</p>

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Claim Terms	Des.	AUO Construction	LGD Construction
dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes	L	<p>dummy conductive patterns cover at least 30% of the region specified by where the dummy conductive patterns are formed; the dummy conductive patterns are situated between the connection pads and the pixel electrodes</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:12-20, esp. 14-20; 1:32-46, esp. 39-44; 2:13-24, esp. 17-21; 3:11-28, esp. 17-22; 3:29-47, esp. 35-41; 3:66-4:2; 5:29-42, esp. 29-33, 38-42; 5:43-53; 5:54-60, esp. 54-57; 5:61-6:6, esp. 5:61-6:1, 6:4-6; 6:7-17, esp. 9-12, 14-17; 6:17-34, esp. 23-27, 30-34; 6:35-47, esp. 35-40; claims 1, 9; Figures 2-4, 5a-5c. May 29, 2003 Office Action, esp. at 2-3. U.S. Patent No. 6,163,356 (Song et al.) 1:55-64; 7:31-63; 8:27-40; 8:41-67. U.S. Patent No. 5,285,301 (Shirahashi et al.) 6:10-18; 13:30-61, esp. 45-61; claims 3, 4; Figures 1, 14, 15.</p> <p>Included is the intrinsic support for disputed terms: "dummy conductive patterns," "a layer of an insulating substrate, having an area," "area," "pixel electrodes".</p>	<p>approximately 30% or more of the area of the layer is made of dummy conductive patterns that are located between the connection pads and an outer edge of the pixel electrodes in the pixel array</p> <p><u>Intrinsic Support</u></p> <p>1:61-67; 3:3-6; 3:16-20; 3:35-40; 5:30-43; 5:46-6:17; 6:29-48; 7:8-18; 7:50-62; Figs. 2-5, 8, 11; App 10/068,500, 5/29/2003, Office Action.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT K
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Claim Terms	Des.	AUO Construction	LGD Construction
pixel electrode	A	<p>an electrode for applying a driving voltage to a liquid crystal display element in a liquid crystal display</p> <p><u>Intrinsic Support</u></p> <p>1:12-20, esp. 14-20; 4:33-41, esp. 38-41; 4:42-50, esp. 46-48; Figures 1-4; May 29, 2003 Office Action, esp. at 2. U.S. Patent No. 5,285,301 (Shirahashi et al.) 8:36-53, esp. 37-39; 9:48-56; Figure 13. U.S. Patent No. 6,163,356 (Song et al.) 1:61-64.</p>	<p>patterns of transparent electrically conductive material that stores charge to drive the liquid crystal material within an individual element of the liquid crystal display device</p> <p><u>Intrinsic Support</u></p> <p>1:12-21; 4:45-51; 6:48-52; Figs 2-5.</p>
each wiring		<p>each individual wiring in the plurality of wiring</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:12-20, esp. 14-20; 1:32-46, esp. 39-44; 3:11-28, esp. 14-16; 3:29-47, esp. 33-34; 4:33-41, esp. 38-41; claims 1, 9; Figures 1-4, 5a-5c, 11, 12a-12b; Application for Patent, esp. at 14; May 29, 2003 Office Action, esp. at 2-3; August 29, 2003 Amendment, esp. at 3, 5.</p> <p>Included is the intrinsic support for the disputed term: "a plurality of wiring arranged on the insulating substrate".</p>	Indefinite

EXHIBIT L

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT L
AU OPTRONICS USP 6,734,944

Claim Terms	Des.	Agreed Constructions
regulates a cell gap between the first and the second substrates	L	maintains a uniform spacing within a manufacturing tolerance between the two substrates in the display region
a spacer	L A	a pillar formed between the first and second substrates to set or maintain the size of the gap between substrates

Disputed Constructions

Claim Terms	Des.	AUO Construction	LGD Construction
at least one of the group consisting of	L	<p>at least one of the characteristics listed as (a) through (e)</p> <p><u>Intrinsic Support</u></p> <p>2:51-54; 6:47-65; claim 4.</p>	<p>Indefinite</p> <p>or</p> <p>means one or more of the limitations selected from (a) to (e)</p> <p><u>Intrinsic Support</u></p> <p>3:55-4:54; 4:56-5:30; 6:47-52; 8:09-20.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT L
AU OPTRONICS USP 6,734,944

Claim Terms	Des.	AUO Construction	LGD Construction
elastic coefficient	A	<p>a value that defines the elasticity of the resin, that is, the resin's ability to change shape or volume in response to force, and then return to its original shape or volume.</p> <p><u>Intrinsic Support</u></p> <p>2:58-3:2; 6:15-24; claim 4; January 16, 2002 Office Action, esp. at 5; August 13, 2002 Office Action, esp. at 3; January 28, 2003 Office Action, esp. at 3-5. U.S. Patent No. 6,299,949 (Shioda et al.) in general, esp.: 3:23-36; 13:1-15; 13:59-67.</p>	Indefinite
Dynamic hardness value (DH)		<p>Defined by the formula in the claim</p> <p><u>Intrinsic Support</u></p> <p>3:54-4:17; 7:27-30; claims 1 and 4; May 16, 2002 Response, esp. at 21-22; November 13, 2002 Response, esp. at 22-23; January 28, 2003 Office Action, esp. at 8-9; June 27, 2003 Office Action, esp. at 10-11; November 28, 2003 Response, esp. at 7-8. U.S. Patent No. 6,299,949 (Shioda et al.) in general, esp.: 14:29-15:16.</p>	<p>Indefinite</p> <p><u>Intrinsic Support</u></p> <p>App 09/558,819, 1/16,2002 Office Action, pages 2-3; App 09/558,819, 5/16/2002 Amendment, pages 21-25; App 09/558,819, 8/13/2002 Office Action, pages 2, 5; App 09/558,819, 11/13/2002 Amendment, pages 22-27; App 09/558,819, 1/28/2003 Office Action, pages 2, 8-11; App 09/558,819, 6/27/2003 Office Action, pages 2, 3, 11-13; App 09/558,819, 11/28/2003 Amendment, pages 7-8.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT L
AU OPTRONICS USP 6,734,944

Claim Terms	Des.	AUO Construction	LGD Construction
Hardness value of plastic deformation (HV)		<p>Defined by the formula in the claim</p> <p><u>Intrinsic Support</u></p> <p>4:18-51; 7:27-30; claims 1 and 4; May 16, 2002 Response, esp. at 21-22; November 13, 2002 Response, esp. at 22-23; January 28, 2003 Office Action, esp. at 8-9; June 27, 2003 Office Action, esp. at 10-11; November 28, 2003 Response, esp. at 7-8. U.S. Patent No. 6,299,949 (Shioda et al.) in general, esp.: 14:29-15:16.</p>	<p>Indefinite</p> <p><u>Intrinsic Support</u></p> <p>App 09/558,819, 1/16,2002 Office Action, pages 2-3; App 09/558,819, 5/16/2002 Amendment, pages 21-25; App 09/558,819, 8/13/2002 Office Action, pages 2, 5; App 09/558,819, 11/13/2002 Amendment, pages 22-27; App 09/558,819, 1/28/2003 Office Action, pages 2, 8-11; App 09/558,819, 6/27/2003 Office Action, pages 2, 3, 11-13; App 09/558,819, 11/28/2003 Amendment, pages 7-8.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT L
AU OPTRONICS USP 6,734,944

Claim Terms	Des.	AUO Construction	LGD Construction
The length of one side of the upper spacer surface		<p>The length of one side of the upper spacer surface, measured using a tangent line parallel to the substrate, at 90% of the height</p> <p><u>Intrinsic Support</u></p> <p>5:49-6:14, and Figs. 2A and 2B; claims 2 and 4.</p>	<p>Indefinite</p> <p>or</p> <p>The distance between two specific points on opposite sides of the spacer (The location of the two points are determined by where a line that runs parallel to the one side and parallel to the substrate intersects the opposite sides. The location of the parallel line is determined by multiplying the height of the spacer by a constant. The height of the spacer is determined by the shortest perpendicular distance measured from the bottom of the spacer to a line tangent to the top of the spacer and parallel to the substrate)</p> <p><u>Intrinsic Support:</u></p> <p>5:51-6:14; Figures 2A, 2B; JP 2000321580A at paragraphs [0009]-[0041]; App 09/558,819, 1/16,2002 Office Action, pages 2-3; App 09/558,819, 5/16/2002 Amendment, pages 21-25; App 09/558,819, 8/13/2002 Office Action, pages 2, 5; App 09/558,819, 11/13/2002 Amendment, pages 22-27; App 09/558,819, 1/28/2003 Office Action, pages 2, 8-11; App 09/558,819, 6/27/2003 Office Action, pages 2, 3, 11-13.</p>

EXHIBIT M

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M
AU OPTRONICS USP 6,778,160

Claim Terms	Des.	Agreed Constructions
a table for storing	L	logic operable to hold data in table form

Disputed Constructions

Claim Terms	Des.	AUO Construction	LGD Construction
video signal	L	<p>a signal comprising video information</p> <p><u>Intrinsic Support</u></p> <p>5:6-14, esp. 6-7, 12-14; 6:51-65, esp. 53-60; 7:17-30, esp. 21-25; claims 1, 3, 4, 6; Figure 1; December 12, 2002 Office Action, esp. at 2-3; March 12, 2003 Amendment, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 2-3, 7-8, 10, 12; March 19, 2004 Notice of Allowability, esp. at 2.</p>	<p>a signal carrying a brightness level from a predetermined range</p> <p><u>Intrinsic Support</u></p> <p>4:47-50; 5:07-15; 5:54-65; 6:27-36; 6:51-7:30; 7:31-45; 10:26-40; 10:57-62; Figs. 1, 2, 8.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M
AU OPTRONICS USP 6,778,160

Claim Terms	Des.	AUO Construction	LGD Construction
a storage for storing the previous brightness level of the video signal input through said input logic	L	<p>memory for storing a previous level of light intensity of a video signal input through input logic</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 3:26-39, esp. 26-30; 5:30-38; claims 8, 12; Figure 1; December 12, 2002 Office Action, esp. at 2-4; March 12, 2003 Amendment, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 3 8, 10-13; March 19, 2004 Notice of Allowability, esp. at 2. U.S. Patent No. 6,333,727 (Mizumaki) Abstract; 3:26-32; 3:39-48; 3:49-55; claims 1, 3, 4.</p> <p>Included is the intrinsic support for disputed terms: "brightness level" and "video signal"</p>	<p>memory that temporarily holds the brightness level of the video signal received from the host through input logic for the previous time increment</p> <p><u>Intrinsic Support</u></p> <p>4:47-50; 5:30-38; 6:11-26; 6:51-7:30; 9:25-39; 9:40-10:14; 10:49-66; Figs. 1, 7; JP 2001-202051A at paragraphs [0010]-[0023].</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M
AU OPTRONICS USP 6,778,160

Claim Terms	Des.	AUO Construction	LGD Construction
determinator for determining an output brightness level	L	<p>logic, such as a circuitry, for determining an output brightness value</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 3:26-39, esp. 30-34; 4:61-5:6, esp. 4:61-67; 6:37-40; 6:66-7:16, esp. 6:66-7:5; claims 4; Figure 1; December 12, 2002 Office Action, esp. at 2-5; March 12, 2003 Amendment, esp. at 1-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 3:9, 12; March 19, 2004 Notice of Allowability, esp. at 2.</p> <p>Included is the intrinsic support for disputed terms: "brightness level," "the next brightness level of the video signal input to said input logic," "video signal," "so as to make a time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level," "ideal quantity of light in a stationary state," "time integration quantity of a brightness level," "substantially equal"</p>	<p>circuit or logic that determines the output brightness level by applying an offset to the next brightness level that is predetermined based on a difference in quantity of light between the actual and ideal response characteristics of the liquid crystal cell</p> <p><u>Intrinsic Support</u></p> <p>1:51-2:12; 4:42-56; 4:61-67; 5:15-30; 5:30-38; 5:51-65; 6:11-26; 6:37-40; 6:51-7:30; 7:31-45; 8:41-61; 9:01-39; 10:26-40; 10:49-66; Figs. 1, 2, 5A, 5B, 6, 7, 8; JP 2001-202051A at paragraphs [0010]-[0023]; App 09/760,131, 12/22/2003, Appeal Brief, pages 2-13.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M
AU OPTRONICS USP 6,778,160

Claim Terms	Des.	AUO Construction	LGD Construction
brightness level	A	<p>level of intensity of light</p> <p><u>Intrinsic Support</u></p> <p>2:26-39, esp. 32-37; 2:50-3:2, esp. 2:63-3:2; 3:15-18; 3:35-37; 3:40-59, esp. 56-59; 3:60-4:7, esp. 3:60-64; 4:42-60; 6:4-6; 8:20-34, esp. 30-34; 8:35-40, esp. 38-40; 10:57-67, esp. 57-62; Figures 2, 4-8, 11; December 12, 2002 Office Action, esp. at 2-5; March 12, 2003 Amendment, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 2-8, 10-12; March 19, 2004 Notice of Allowability, esp. at 2. U.S. Patent No. 6,333,727 (Mizumaki) Abstract; 3:26-32; 3:33-38; 3:39-48; 3:49-55; 3:56-61; 4:7-13; 4:14-22; 4:23-36; 9:7-19, esp. 13-18; claims 1-5. U.S. Patent No. 6,326,938 (Ishida et al.), esp. 1:33-50, esp. 40-42. U.S. Patent No. 5,956,014 (Kuriyama et al.), esp. 1:55-62.</p>	<p>gray scale value or luminance value</p> <p><u>Intrinsic Support</u></p> <p>4:47-50; 5:54-65; 6:51-7:30; 7:31-45; 9:25-39; 9:40-10:14; 10:26-40; 10:57-62; Figures 1, 2, 7, 8.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M
AU OPTRONICS USP 6,778,160

Claim Terms	Des.	AUO Construction	LGD Construction
the next brightness level of the next video signal input to said input logic	L	<p>plain meaning</p> <p><u>Intrinsic Support</u></p> <p>Summary of the Invention and Detailed Description of the Invention, generally; 6:11-27, esp. 11-17; 6:37-40; 6:66-7:17, esp. 7:13-15; claim 12; Figures 7, 9, 10; December 12, 2002 Office Action, esp. at 2-5; March 12, 2003 Amendment, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 2 8, 10-13; March 19, 2004 Notice of Allowability, esp. at 2. U.S. Patent No. 6,333,727 (Mizumaki) Abstract; 3:26-32; 3:39-48; 3:49-55; 4:14 22; 4:23-36; 7:4-22; 8:23-37; claims 1, 3, 4.</p> <p>Included is the intrinsic support for the disputed term: "video signal"</p>	<p>the brightness level of the video signal received from the host input to the input logic for the next time increment</p> <p><u>Intrinsic Support</u></p> <p>4:47-50; 5:30-38; 6:11-26; 6:51-7:30; 9:25-39; 9:40-10:14; 10:49-66; Figures 1, 7; JP 2001-202051A at paragraphs [0010]-[0023].</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M
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Claim Terms	Des.	AUO Construction	LGD Construction
so as to make a time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level	L	<p>So as to make a time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level; the next brightness level is the brightness level that immediately follows the previous brightness level.</p> <p><u>Intrinsic Support</u></p> <p>8:35-40; 9:8-25, esp. 8-23; claims 4, 5, 12; Figures 2, 4-8, 11; December 12, 2002 Office Action, esp. at 2-5; March 12, 2003 Amendment, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 2 13; March 19, 2004 Notice of Allowability, esp. at 2.</p> <p>Included is the intrinsic support for disputed terms: "time integration quantity of a brightness level," "substantially equal," "ideal quantity of light in a stationary state," "the next brightness level of the next video signal input to said input logic"</p>	<p>so that the quantity of light based on the actual response characteristic of the liquid crystal cell is substantially equal to the quantity of light based on the ideal response characteristic of the liquid crystal cell when the liquid crystal cell is provided with the next brightness level during the next time increment and the previous brightness level before and after the next time increment</p> <p><u>Intrinsic Support</u></p> <p>1:39-43; 1:51-2:12; 4:42-56; 4:61-67; 5:15-30; 5:16-22; 5:66-6:06; 6:11-26; 6:51-7:30; 7:31-45; 8:35-40; 8:41-61; 9:01-39; 10:26-40; 10:49-66; Figures 1, 2, 4, 5A, 5B, 6, 7, 8; JP 2001-202051A at paragraphs [0010]-[0023]; App 09/760,131, 12/22/2003, Appeal Brief, pages 2-13.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M
AU OPTRONICS USP 6,778,160

Claim Terms	Des.	AUO Construction	LGD Construction
ideal quantity of light in a stationary state	A	<p>the quantity of light emitted by a pixel during one time increment when the pixel is in a non-changing state</p> <p><u>Intrinsic Support</u></p> <p>4:42-60, esp. 42-47; 6:11-27, esp. 14-19; 8:35-40; claims 4, 12; Figures 2, 4-6, 8, 11; December 12, 2002 Office Action, esp. at 2-3; March 12, 2003 Amendment, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 3 4, 7-8, 12; March 19, 2004 Notice of Allowability, esp. at 2.</p>	<p>quantity of light based on the ideal response characteristic of the liquid crystal cell when the liquid crystal cell is provided with the next brightness level during the next time increment and the previous brightness level before and after the next time increment</p> <p><u>Intrinsic Support</u></p> <p>1:39-43; 4:42-56; 5:66-6:06; 7:31-45; 8:35-40; 8:41-61; 9:01-39; 10:26-40; 10:49-66; Figures 2, 4, 5A, 5B, 6, 7, 8; JP 2001-202051A at paragraphs [0010]-[0023].</p>
image displaying liquid crystal cell	L	<p>an image display element with a liquid crystal</p> <p><u>Intrinsic Support</u></p> <p>1:39-45, esp. 39-41; 3:40-59, esp. 40-44; 7:17-30, esp. 25-28; Figure 1; December 12, 2002 Office Action, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 9:12.</p>	<p>an image display element with a liquid crystal that has the ideal response characteristic at the maximum brightness change given the predetermined range of brightness levels</p> <p><u>Intrinsic Support</u></p> <p>2:25-3:02; 5:40-45; 6:51-7:30; 7:31-45; 7:66-8:25; 10:26-40; Figures 1, 2, 3, 7, 8.</p>

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Claim Terms	Des.	AUO Construction	LGD Construction
first brightness information for an input pixel	L	<p>a level of light intensity for an input pixel</p> <p><u>Intrinsic Support</u></p> <p>Summary of the Invention and Detailed Description of the Invention, generally; Abstract; 3:27-39, esp. 27-29; 4:61-5:6, esp. 4:61-64; 6:66-7:16, esp. 7:13-15; claims 1, 13; Figures 7, 9, 10; December 12, 2002 Office Action, esp. at 2:4; March 12, 2003, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 3-9, 12, 13; March 19, 2004 Notice of Allowability, esp. at 2. U.S. Patent No. 6,333,727 (Mizumaki) Abstract; 3:26-32; 3:39-48; 3:49-55; 4:14-22; 4:23-36; 7:4-22; 8:23-37; claims 1, 3, 4.</p> <p>Included is the intrinsic support for disputed terms: "pixel" and "brightness level".</p>	<p>the brightness level of an input signal for a pixel</p> <p><u>Intrinsic Support</u></p> <p>4:47-50; 5:07-15; 5:30-38; 5:54-65; 6:11-26; 6:27-36; 6:51-7:30; 7:31-45; 9:25-39; 9:40-10:14; 10:26-40; 10:49-66; Figures 1, 2, 7, 8; JP 2001-202051A at paragraphs [0010]-[0023].</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M
AU OPTRONICS USP 6,778,160

Claim Terms	Des.	AUO Construction	LGD Construction
pixel	L	<p>abbreviation for "picture element"</p> <p><u>Intrinsic Support</u></p> <p>1:39-45, esp. 43-45; 2:44-49, esp. 44-47; 2:50-3:2, esp. 50-54; 3:40-59, esp. 40-50; 3:60-4:7, esp. 3:64-4:4; 4:42-60, esp. 42-47; 5:51-65, esp. 54-65; 5:67-6:3, claims 4, 7, 9, 10; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 2:7, 10-12. U.S. Patent No. 6,333,727 (Mizumaki) Abstract; 2:23-33, esp. 23-27; 3:26-32; 3:39-48; 3:49-55; 4:14-22; 4:23-36; 7:4-22; 7:46-60, esp. 56-60; 8:23-37, esp. 23-25; claims 1, 3, 4; Figure 6. U.S. Patent No. 5,483,634 (Hasegawa) 4:23-57, esp. 30-36. U.S. Patent No. 6,064,359 (Lin et al.) 1:12 18, esp. 12-15; 1:21-34, esp. 28-31; 1:35-58, esp. 46-49; 4:60-5:4, esp. 1-4.</p>	<p>an image display element with a liquid crystal that has the ideal response characteristic at the maximum brightness change</p> <p><u>Intrinsic Support</u></p> <p>2:25-3:02; 5:40-45; 6:51-7:30; 7:31-45; 7:66-8:25; 10:26-40; Figures 1, 2, 3, 7, 8.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M
AU OPTRONICS USP 6,778,160

Claim Terms	Des.	AUO Construction	LGD Construction
frame buffer	L	<p>storage for video information contained in a frame</p> <p><u>Intrinsic Support</u></p> <p>5:30-38, esp. 30-36; 6:11-27; 6:66-7:16, esp. 7:5-10; claims 8, 12, 13; Figure 1; December 12, 2002 Office Action, esp. at 2 5; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 3-8,10-13; March 19, 2004 Notice of Allowability, esp. at 2. U.S. Patent No. 5,347,294 (Usui et al.) 4:64-67, esp. 64-65; 9:28-32, esp. 28-31; 12:53-57, esp. 53-55, U.S. Patent No. 6,333,727 (Mizumaki) 3:26-32; 5:10-18, esp. 15-18; 6:8-11. U.S. Patent No. 5,483,634 (Hasegawa) 4:26-28, esp. 26-27.</p>	<p>a memory circuit or device that temporarily holds brightness levels for all pixels that form one complete picture on the liquid crystal display</p> <p><u>Intrinsic Support</u></p> <p>1:43-45; 5:31-33; 6:11-26; 6:51-7:30; 9:25-39; 9:40-10:14; 10:49-66; Figures 1, 7.</p>

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Claim Terms	Des.	AUO Construction	LGD Construction
second brightness information for the next input pixel	L	<p>a level of light intensity for a next input pixel</p> <p><u>Intrinsic Support</u></p> <p>Summary of the Invention and Detailed Description of the Invention, generally; Abstract; 3:26-39, esp. 30-37; 4:61-5:6, esp. 4:61-67; 6:66-7:16, esp. 7:13-15; claims 2, 12; Figures 7, 9, 10; December 12, 2002 Office Action, esp. at 2-4; March 12, 2003, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 3-9, 12, 13; March 19, 2004 Notice of Allowability, esp. at 2. U.S. Patent No. 6,333,727 (Mizumaki) Abstract; 3:26-32; 3:39-48; 3:49-55; 4:14-22; 4:23-36; 7:4-22; 8:23-37; claims 1, 3, 4.</p> <p>Included is the intrinsic support for disputed terms: "pixel" and "brightness level".</p>	<p>the brightness level for the next frame of the input signal for the pixel</p> <p><u>Intrinsic Support</u></p> <p>4:47-50; 5:30-38; 6:11-26; 6:51-7:30; 9:25-39; 9:40-10:14; 10:49-66; Figures 1, 7; JP 2001-202051A at paragraphs [0010]-[0023].</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M
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Claim Terms	Des.	AUO Construction	LGD Construction
an offset for making the time integration quantity of a brightness change substantially equal to an ideal light quantity which is the brightness in a stationary state to said second brightness information	L	<p>a modification of the second brightness information for making the time integration quantity of the brightness change substantially equal to an ideal light quantity which is the brightness in a stationary state</p> <p><u>Intrinsic Support</u></p> <p>2:4-12, esp. 4-10; 5:15-21; 5:22-29, esp. 27-29; 9:1-7; 9:8-24, esp. 8-23; 9:40-63; claims 4, 5; Figures 2, 7-8; December 12, 2002 Office Action, esp. at 2-5; March 12, 2003, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 2-13; March 19, 2004 Notice of Allowability, esp. at 2.</p> <p>Included is the intrinsic support for disputed terms: "time integration quantity of a brightness level," "substantially equal," "ideal light quantity which is the brightness in a stationary state," "brightness level".</p>	<p>a value predetermined based on difference in quantity of light between the actual and ideal response characteristics of the pixel so that the quantity of light based on the actual response characteristic of the pixel to be substantially equal to the quantity of light based on the ideal response characteristic of the pixel when the pixel is provided with the second brightness level during the next frame and the first brightness level before and after the next frame</p> <p><u>Intrinsic Support</u></p> <p>1:39-43; 1:51-2:12; 4:42-56; 4:61-67; 5:15-30; 5:30-38; 5:51-65; 5:66-6:06; 6:11-26; 6:37-40; 6:51-7:30; 7:31-45; 8:35-40; 8:41-61; 9:01-39; 10:26-40; 10:49-66; Figures 1, 2, 4, 5A, 5B, 6, 7, 8; JP 2001-202051A at paragraphs [0010]-[0023]; App 09/760,131, 12/22/2003, Appeal Brief, pages 2-13.</p>

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AU OPTRONICS USP 6,778,160

Claim Terms	Des.	AUO Construction	LGD Construction
time integration quantity of a brightness change	A	<p>a quantity of light equal to the actual brightness level output through a liquid crystal, summed over a time period including the rise and fall response time of the liquid crystal</p> <p><u>Intrinsic Support</u></p> <p>4:42-60, esp. 53-56; 8:20-34, esp. 30-34; 11:1-9, esp. 1-4; claims 5, 11; Figures 4-6, 11; December 12, 2002 Office Action, esp. at 2:5; March 12, 2003, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 3-9, 12; March 19, 2004 Notice of Allowability, esp. at 2.</p> <p>Included is the intrinsic support for the disputed term: "brightness level".</p>	<p>Indefinite</p> <p>or</p> <p>quantity of light based on the actual response characteristic of the liquid crystal cell when the liquid crystal cell is provided with the next brightness level during the next time increment and the previous brightness level before and after the next time increment</p> <p><u>Intrinsic Support</u></p> <p>1:39-43; 4:42-56; 4:61-5:06; 5:16-22; 5:66-6:06; 7:31-45; 8:41-61; 9:01-39; 10:26-40; 10:49-66; Figures 2, 5A, 5B, 6, 7, 8; JP 2001-202051A at paragraphs [0010]-[0023].</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M
AU OPTRONICS USP 6,778,160

Claim Terms	Des.	AUO Construction	LGD Construction
ideal light quantity which is the brightness in a stationary state	A	<p>the quantity of light emitted by a pixel during one time increment when the pixel is in a non-changing state</p> <p><u>Intrinsic Support</u></p> <p>4:42-60, esp. 42-47; 6:11-27, esp. 11-19; 8:35-40; 10:49-56, esp. 49-52; claims 4, 12; Figures 2, 4-6, 8, 11; December 12, 2002 Office Action, esp. at 2:3; March 12, 2003, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 3-4, 7-8, 12; March 19, 2004 Notice of Allowability, esp. at 2.</p> <p>Included is the intrinsic support for the disputed term: "brightness level".</p>	(see above term)

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M
AU OPTRONICS USP 6,778,160

Claim Terms	Des.	AUO Construction	LGD Construction
substantially equal		<p>a level that is not completely the same but can be accepted as a substantially equal level</p> <p><u>Intrinsic Support</u></p> <p>4:42-60, esp. 56-58; 8:41-61, esp. 45-47; 9:26-39, esp. 32-35; claim 4; Figures 4-6, 11; December 12, 2002 Office Action, esp. at 2-3; March 12, 2003, esp. at 1-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 2-10, 12; March 19, 2004 Notice of Allowability, esp. at 2. U.S. Patent No. 6,333,727 (Mizumaki) Abstract; 3:33-38; 3:56-61; 4:7-13; 4:23-36; 7:4-22; 8:38-57; 9:7-19; claims 1-5.</p>	<p>Indefinite</p> <p>or</p> <p>A level which is not completely the same but can be accepted as a substantially equivalent level, and includes a level which is closer to an ideal quantity of light than no preventive measures are taken.</p> <p><u>Intrinsic Support</u></p> <p>4:56-60.</p>

EXHIBIT N

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT N
AU OPTRONICS USP 6,976,781

Disputed Constructions

Claim Terms	Des.	AUO Construction	LGD Construction
on outer surfaces of said first edge a plurality of first hooks are formed to protrude outwardly	L	<p>an outer surfaces of said first edge a plurality of first protruding structures, intended to be inserted into a hole for the purpose of fastening one element to another, are formed to protrude outwardly</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term “hooks”</p>	<p>two or more protrusions that are part of the frame and that extend outwardly from the first edge for fastening the frame to the bezel</p> <p><u>Intrinsic Support</u></p> <p>1:44-2:25; 2:28-32; 3:4-21, 31-42, 49-66; 4:16-22, 26-33; Figs. 1, 2, 3, 4 and 5; App 10/446,103, 9/28/2004 Office Action, pages 4-8; App 10/446,103, 1/28/2005 Response, pages 5, 6, 8-10; 13-14; App 10/446,103, 3/8/2005 Final Office Action, pages 3-5, 7-9; App 10/446,103, 6/8/2005 Response, page 5; App 10/446,103, 6/27/2005 Notice of Allowability, pages 2-3.</p>
hooks	A	<p>Any protruding structure intended to be inserted into a hole for the purpose of fastening one element to another</p> <p><u>Intrinsic Support</u></p> <p>1:44-53; 1:54-63; 3:4-13; 3:14-21; Figures 1-5, including those portions of the specification discussing the same; U.S. Patent No.: 5,570,267 (Ma): 2:3-45, esp. 2:41-42, and Figure 2, element 32.</p>	(see above term)

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AU OPTRONICS USP 6,976,781

Claim Terms	Des.	AUO Construction	LGD Construction
on outer surfaces of said second sidewall a plurality of second hooks are formed to protrude outwardly	L	<p>on outer surfaces of said second sidewall a plurality of second protruding structures, intended to be inserted into a hole for the purpose of fastening one element to another, are formed to protrude outwardly</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term "hooks."</p>	<p>two or more protrusions that are part of the bezel and that extend outwardly from the second sidewall for fastening the bezel to the frame</p> <p><u>Intrinsic Support</u></p> <p>1:44-2:25, 28-32; 3:4-21, 31-42, 49-66; 4:16-22, 26-33; Figs. 1, 2, 3, 4 and 5; App 10/446,103, 9/28/2004 Office Action, pages 4-8; App 10/446,103, 1/28/2005 Response, pages 5, 6, 8-10; 13-14; App 10/446,103, 3/8/2005 Final Office Action, pages 3-5, 7-9; App 10/446,103, 6/8/2005 Response, page 5; App 10/446,103, 6/27/2005 Notice of Allowability, pages 2-3.</p>
as said frame is mounted onto said bezel	L	<p>during the process of mounting the frame onto the bezel</p> <p><u>Intrinsic Support</u></p> <p>3:22-42, esp. 3:34-42; January 28, 2005 Amendment, esp. at 8, amendment to Claim 1 ("Listing of Current Claims")</p>	<p>at the same time when the frame and bezel are joined</p> <p><u>Intrinsic Support</u></p> <p>1:44-2:25; 2:28-32; 3:4-21, 31-42, 49-66; 4:16-22, 26-33; Figs. 1, 2, 3, 4 and 5; App 10/446,103, 9/28/2004 Office Action, pages 4-8; App 10/446,103, 1/28/2005 Response, pages 5, 6, 8-10; 13-14; App 10/446,103, 3/8/2005 Final Office Action, pages 3-5, 7-9; App 10/446,103, 6/8/2005 Response, page 5; App 10/446,103, 6/27/2005 Notice of Allowability, pages 2-3.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT N
AU OPTRONICS USP 6,976,781

Claim Terms	Des.	AUO Construction	LGD Construction
bezel	A	<p>A frame, typically made of metal</p> <p><u>Intrinsic Support</u></p> <p>1:30-43, esp. 1:33 and Figure 1, element 110; 2:33-50, esp. 2:38-39; 3:14-21, esp. 3:14-18 and Figure 4; 4:7-22, esp. 4:7-9; U.S. Patent No.: 6,170,956 (Rumsey et al.): 5:58-65, esp. 5:61 and Figure 2, element 12; 10:34-11:10, esp. 11:6 and Figure 17, element 117; 12:15-44, esp. 12:15-17 and Figures 17 and 18, element 117; U.S. Patent No.: 6,386,722 (Okumura): 1:20-34, esp. 1:26-27; 3:53-65, esp. 3:53-55, 3:59-60, and Figure 1, element 40.</p>	<p>the outermost back cover for the backlight module</p> <p><u>Intrinsic Support</u></p> <p>1:30-43; 1:66-2:7; 3:14-31; 4:7-9; Figs. 1, 2, 3, 4 and 5.</p>

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AU OPTRONICS USP 6,976,781

Claim Terms	Des.	AUO Construction	LGD Construction
on outside surfaces of said first edge first hooks are formed to protrude outwardly	L	<p>on outside surfaces of said first edge first protruding structures, intended to be inserted into a hole for the purpose of fastening one element to another, are formed to protrude outwardly</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term “hooks.”</p>	<p>two or more protrusions that are part of the frame and that extend outwardly from the first edge for fastening the frame to the bezel</p> <p><u>Intrinsic Support</u></p> <p>1:44-2:25; 2:28-32; 3:4-21, 31-42, 49-66; 4:16-22, 26-33; Figs. 1, 2, 3, 4 and 5; App 10/446,103, 9/28/2004 Office Action, pages 4-8; App 10/446,103, 1/28/2005 Response, pages 5, 6, 8-10; 13-14; App 10/446,103, 3/8/2005 Final Office Action, pages 3-5, 7-9; App 10/446,103, 6/8/2005 Response, page 5; App 10/446,103, 6/27/2005 Notice of Allowability, pages 2-3.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT N
AU OPTRONICS USP 6,976,781

Claim Terms	Des.	AUO Construction	LGD Construction
on outside surfaces of said fourth edge second hooks are formed to protrude outwardly	L	<p>on outside surfaces of said fourth edge second protruding structures, intended to be inserted into a hole for the purpose of fastening one element to another, are formed to protrude outwardly</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term “hooks.”</p>	<p>two or more protrusions that are part of the frame and that extend outwardly from the fourth edge for fastening the frame to the bezel</p> <p><u>Intrinsic Support</u></p> <p>1:44-2:25; 2:28-32; 3:4-21, 31-42, 49-66; 4:16-22, 26-33; Figs. 1, 2, 3, 4 and 5; App 10/446,103, 9/28/2004 Office Action, pages 4-8; App 10/446,103, 1/28/2005 Response, pages 5, 6, 8-10; 13-14; App 10/446,103, 3/8/2005 Final Office Action, pages 3-5, 7-9; App 10/446,103, 6/8/2005 Response, page 5; App 10/446,103, 6/27/2005 Notice of Allowability, pages 2-3.</p>

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AU OPTRONICS USP 6,976,781

Claim Terms	Des.	AUO Construction	LGD Construction
on outer surfaces of said second sidewall a plurality of first hooks are formed to protrude outwardly	L	<p>on outer surfaces of said second sidewall a plurality of first protruding structures, intended to be inserted into a hole for the purpose of fastening one element to another, are formed to protrude outwardly</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term “hooks.”</p>	<p>two or more protrusions that are part of the bezel and that extend outwardly from the second sidewall for fastening the bezel to the frame</p> <p><u>Intrinsic Support</u></p> <p>1:44-2:25; 2:28-32; 3:4-21, 31-42, 49-66; 4:16-22, 26-33; Figs. 1, 2, 3, 4 and 5; App 10/446,103, 9/28/2004 Office Action, pages 4-8; App 10/446,103, 1/28/2005 Response, pages 5, 6, 8-10; 13-14; App 10/446,103, 3/8/2005 Final Office Action, pages 3-5, 7-9; App 10/446,103, 6/8/2005 Response, page 5; App 10/446,103, 6/27/2005 Notice of Allowability, pages 2-3.</p>

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AU OPTRONICS USP 6,976,781

Claim Terms	Des.	AUO Construction	LGD Construction
on outer surfaces of said first edge a plurality of second hooks are formed to protrude outwardly	L	<p>on outer surfaces of said first edge a plurality of second protruding structures, intended to be inserted into a hole for the purpose of fastening one element to another, are formed to protrude outwardly</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term “hooks.”</p>	<p>two or more protrusions that are part of the frame and that extend outwardly from the first edge for fastening the frame to the bezel</p> <p><u>Intrinsic Support</u></p> <p>1:44-2:25; 2:28-32; 3:4-21, 31-42, 49-66; 4:16-22, 26-33; Figs. 1, 2, 3, 4 and 5; App 10/446,103, 9/28/2004 Office Action, pages 4-8; App 10/446,103, 1/28/2005 Response, pages 5, 6, 8-10; 13-14; App 10/446,103, 3/8/2005 Final Office Action, pages 3-5, 7-9; App 10/446,103, 6/8/2005 Response, page 5; App 10/446,103, 6/27/2005 Notice of Allowability, pages 2-3.</p>
simultaneously said second edge is disposed onto outside surfaces of said second sidewall, and said first hooks are inserted and engaged in said second holes for fastening said frame and said bezel	L	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>3:22-42, esp. 3:34-42; January 28, 2005 Amendment, esp. at 8 , amendment to Claim 1 ("Listing of Current Claims")</p>	<p>the first hooks are inserted and engaged with the second holes at the same time the second hooks are inserted and engaged with the first holes to join the frame and bezel</p> <p><u>Intrinsic Support</u></p> <p>1:44-2:25; 2:28-32; 3:4-21, 31-42, 49-66; 4:16-22, 26-33; Figs. 1, 2, 3, 4 and 5.</p>

EXHIBIT O

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT O
AU OPTRONICS USP 7,090,506

Disputed Constructions

Claim Terms	Des.	AUO Construction	LGD Construction
a first flexible printed circuit board, electrically connecting the display module and the system	L	<p>a first printed circuit made on a flexible film that electrically connects the display module and the system</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:12-21, and Fig. 1; 1:25-34; 1:60-2:5, esp. 1:65-67, and Fig. 2; 2:38-48, and Figs 4a and 4b; claims 1, 5, 9, 13, 17 and 20; October 28, 2005 Office Action, esp. at 2-3; February 14, 2006 Office Action, esp. at 2; May 10, 2006 Response, esp. at 10. U.S. Patent Application Publication No. 2005/0185127 A1 (Fujiyama et al.) in general, esp. 0026 and Figs. 1, 5.</p>	<p>a first flexible film with conductive patterns printed on its surface that electrically connects the display module and the system</p> <p><u>Intrinsic Support</u></p> <p>1:25-35; 1:60-2:25, 40-9, 58-66; Figs. 2, 3a, 3b; 4a, 4b; App 10/921,462, 2/14/06 Office Action, pages 2-3; App 10/921,462, 5/10/06 Response, pages 9-14.</p>

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Claim Terms	Des.	AUO Construction	LGD Construction
display module	A	<p>an LCD module</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:7-10; 1:11-21, and Fig. 1; 1:25-34; 1:60-2:15, and Fig. 2; 2:61-64; 3:2-6; 3:7-15; claims 1, 5-9, 13-17, and 20-23; October 28, 2005 Office Action, esp. at 2-3; February 14, 2006 Office Action, esp. at 2; May 10, 2006 Response, esp. at 10. U.S. Patent Application Publication No. 2005/0185127 A1 (Fujiyama et al.) in general, esp.: Abstract; 0003; 0008; 0018 and Fig. 1. U.S. Patent No. 5,684,550 (Shibata et al.) in general, esp.: Abstract; 3:63-67 and Figs. 23, 24(a)-24(E); 17:16-47 and Figs. 23-39.</p>	<p>an assembly that includes an LCD panel, a touch panel and a light source</p> <p><u>Intrinsic Support</u></p> <p>1:13-21, 25-35, 61-65; 2:58-64; 3:2-6; Figs. 1 and 2.</p>

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AU OPTRONICS USP 7,090,506

Claim Terms	Des.	AUO Construction	LGD Construction
a second flexible printed circuit board, electrically connecting the display module and the first flexible printed circuit board	L	<p>a second printed circuit made on a flexible film that electrically connects the display module and the first printed circuit made on a flexible film</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:12-21, and Fig. 1; 1:25-34; 1:60-2:15, esp. 2:6-15, and Fig. 2; 2:38-57, and Figs 4a and 4b; claims 1, 6, 7, 9, 14, 15, 17, 21, and 22; October 28, 2005 Office Action, esp. at 2-3; February 14, 2006 Office Action, esp. at 2; May 10, 2006 Response, esp. at 10. U.S. Patent Application Publication No. 2005/0185127 A1 (Fujiyama et al.) in general, esp. 0026 and Figs. 1, 5.</p>	<p>a second flexible film with conductive patterns printed on its surface that electrically connects the display module and the first flexible film</p> <p><u>Intrinsic Support</u></p> <p>1:25-35; 1:60-2:25, 40-9, 58-66; Figs. 2, 3a, 3b; 4a, 4b; App 10/921,462, 2/14/06 Office Action, pages 2-3; App 10/921,462, 5/10/06 Response, pages 9-14.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT O
AU OPTRONICS USP 7,090,506

Claim Terms	Des.	AUO Construction	LGD Construction
the first and second flexible printed circuit boards are joined by hot bar soldering	L	<p>the first and second printed circuits made on flexible film are joined by a soldering process where the solder and flux are applied to the contact area and the contact area is heated with a bar to melt the solder</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:25-34, esp. 1:30-34; 1:60-2:15, and Fig. 2; 2:16-37, and Figs. 2, 3a, and 3b; 2:64-67; claim 1; October 28, 2005 Office Action, esp. at 2-3. U.S. Patent Application Publication No. 2005/0185127 A1 (Fujiyama et al.) in general, esp.: 0021, 0045, and Fig. 1.</p>	<p>both flexible printed circuit boards are connected to each other by a soldering process where the circuit boards are heated with a bar to melt the solder at multiple points simultaneously along each circuit board while pressure is applied to the connection</p> <p><u>Intrinsic Support</u></p> <p>1:25-35; 2:6-37, 46-49, 58-67; Figs. 2, 3a, 3b; App 10/921,462, 2/14/06 Office Action, pages 2-3; App 10/921,462, 5/10/06 Response, pages 9-14; .App 10/921,462, 5/19/06 Notice of Allowability, page 2.</p>
the first and second flexible printed circuit boards are joined by anisotropic conductive film (ACF) bonding	L	<p>both flexible circuit boards are connected to each other by a material that is conductive in one direction after being pressed between the two circuit boards</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:25-34, esp. 1:30-34; 2:40-57, and Figs. 2, 4a, and 4b; 2:64-67; claim 9; October 28, 2005 Office Action, esp. at 2-3. U.S. Patent Application Publication No. 2005/0185127 A1 (Fujiyama et al.) in general, esp.: 0042, 0055, and Figs. 1, 5.</p>	<p>both flexible printed circuit boards are connected to each other by a process where a material that is conductive in one direction is pressed between the two circuit boards</p> <p><u>Intrinsic Support</u></p> <p>1:25-35; 2:6-20, 40-49, 58-67; Figs. 2, 4a, 4b; App 10/921,462, 2/14/06 Office Action, pages 2-3; App 10/921,462, 5/10/06 Response, pages 9-14; .App 10/921,462, 5/19/06 Notice of Allowability, page 2.</p>

EXHIBIT P

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT P
AU OPTRONICS USP 7,101,069

Disputed Constructions

Claim Terms	Des.	AUO Construction	LGD Construction
a fitting portion	L	<p>a structure for accommodating an illumination tube</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:43-52, esp. 44-45; 1:57-65, esp. 62-65; 2:39-43; 2:50-54; 2:55-3:2, esp. 2:63-3:2; 3:9-14, esp. 9-10; claims 1, 3, 7, 8, 16-18; Figures 3, 4, 5A-5G; May 3, 2005 Office Action, esp. at 2-3; January 9, 2006 Response After Final Rejection, esp. at 6.</p>	<p>the portion of the support designed to hold an illumination tube</p> <p><u>Intrinsic Support</u></p> <p>1:64-65; 2:41-43; 2:50-53; 2:62-3:3; Abstract; Figs. 3, 5A-G; App 10/613,493, 1/9/06 Response, pages 2, 4-7; App 10/613,493, 4/20/06 Notice of Allowability, page 2.</p>
comprises two side walls extending upwardly and separately	L	<p>having at least two sidewalls extending upwardly and separately</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:43-52, esp. 44-45; 1:57-65, esp. 62-65; 2:39-43; 2:50-54; 2:55-3:2, esp. 2:63-64; 3:9-14; claims 1, 7, 8, 16-18; Figures 3, 4, 5A-5G; May 3, 2005 Office Action, esp. at 2; October 20, 2005 Office Action, esp. at 2-3; January 9, 2006 Response After Final Rejection, esp. at 6; April 20, 2006 Notice of Allowability. JP 2001-210126, esp. ¶¶ 0012, 0014, 0016-0020, 0030, 0038 and Figures 4-5.</p>	<p>includes two upright structures that are spaced apart and that are designed to hold the illumination tube</p> <p><u>Intrinsic Support</u></p> <p>2:44-9, 55-61; Figs. 5B, 5C, 5F, and 5G; App 10/613,493, 1/9/06 Response, pages 2, 4-7; App 10/613,493, 4/20/06 Notice of Allowability, page 2.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT P
AU OPTRONICS USP 7,101,069

Claim Terms	Des.	AUO Construction	LGD Construction
has two side walls extending upwardly and separately	L	<p>having two sidewalls extending upwardly and separately</p> <p><u>Intrinsic Support</u></p> <p>Figures 3, 4, 5A-5G; claims 1, 7, 8, 16-18; January 9, 2006 Response After Final Rejection, esp. at 6; April 20, 2006 Notice of Allowability. JP 2001-210126, esp. ¶¶ 0012, 0014, 0016-0020, 0030, 0038 and Figures 4-5.</p>	<p>has two upright structures that are spaced apart and that are designed to hold the illumination tube</p> <p><u>Intrinsic Support</u></p> <p>2:44-9, 55-61; Figs. 5B, 5C, 5F, and 5G; App 10/613,493, 1/9/06 Response, pages 2, 4-7; App 10/613,493, 4/20/06 Notice of Allowability, page 2.</p>

EXHIBIT Q

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT Q
AU OPTRONICS USP 7,125,157

Disputed Constructions

Claim Terms	Des.	AUO Construction	LGD Construction
a first supporting portion, disposed on the frame	L	<p>A first supporting portion, disposed on the frame, wherein the term "supporting portion" has the meaning proposed by AUO (i.e. any structure protruding from the frame (including but not limited to a cylinder or a cuboid) intended to support the optical film).</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term "supporting portion."</p>	<p>a first projection from the frame that supports the film when the backlight is in a first position</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 2:1-8; 4:18-24; 4:48-64; 5:17-22; 5:45-6:8; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>
supporting portion	A	<p>Any structure protruding from the frame, (including but not limited to a cylinder or a cuboid) intended to support the optical film</p> <p><u>Intrinsic Support</u></p> <p>2:61-62; 2:66-3:4; 3:5-3:12; 4:17-24, esp. 4:17-21 and Figures 2A and 2B; 6:4-8, esp. 6:4-6 and Figures 3A and 3B; 6:31-42, esp. 6:40-42 and Figure 3C; 7:39-45 and Figures 4A – 4D; claim 10, 22.</p> <p>Included is the intrinsic support for disputed term "constraining portion."</p>	(see above)

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT Q
AU OPTRONICS USP 7,125,157

Claim Terms	Des.	AUO Construction	LGD Construction
a second supporting portion, further disposed on the frame	L	<p>A second supporting portion, further disposed on the frame, wherein the term "supporting portion" has the meaning proposed by AUO (i.e. any structure protruding from the frame (including but not limited to a cylinder or a cuboid) intended to support the optical film).</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term "supporting portion."</p>	<p>a second projection from the frame that supports the film when the backlight is rotated from the first position</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 4:48-64; 5:36-6:8; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>
a first constraining portion	L	<p>A first constraining portion, wherein the term "constraining portion" has the meaning proposed by AUO (i.e. any formation on or in the optical film (including but not limited to a hole or a groove) intended to restrict the movement range of the film).</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term "constraining portion."</p>	<p>a first passage through the film that has a gap in the gravity acting direction after receiving a supporting portion</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 2:66-3:19; 5:39-6:3; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 1/25/06 Office Action, pages 8-9; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT Q
AU OPTRONICS USP 7,125,157

Claim Terms	Des.	AUO Construction	LGD Construction
constraining portion	A	<p>Any formation on or in the optical film (including but not limited to a hole or groove) intended to restrict the movement range of the film</p> <p><u>Intrinsic Support</u></p> <p>2:27-30; 2:63-65; 4:7-16, esp. 4:13-15 and Figure 2A; 6:47-49; 7:22-33, esp. 7:28-29 and Figure 3C; claims 2, 11, 17.</p> <p>Included is the intrinsic support for disputed term “supporting portion.”</p>	<p>a passage through the film that has a gap in the gravity acting direction after receiving a supporting portion</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 2:66-3:19; 5:45-6:3; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 1/25/06 Office Action, pages 8-9; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>
a second constraining portion	L	<p>A second constraining portion, wherein the term "constraining portion" has the meaning proposed by AUO (i.e. any formation on or in the optical film (including but not limited to a hole or a groove) intended to restrict the movement range of the film).</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term “constraining portion.”</p>	<p>a second passage through the film that has a gap in the gravity acting direction after receiving a supporting portion</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 2:66-3:19; 5:36-6:3; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 1/25/06 Office Action, pages 8-9; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT Q
AU Optronics USP 7,125,157

Claim Terms	Des.	AUO Construction	LGD Construction
disposed in a first position	L	<p>an initial position of a liquid crystal display unit.</p> <p><u>Intrinsic Support</u></p> <p>2:12-26, esp. 2:19-25; 2:52-60; 2:66-3:4; 4:37-42; 4:48-56, esp. Figure 3A; 5:37-54, esp. 5:39-44 and Figure 3A; 6:14-30, esp. 6:22-27 and Figure 3C; 7:22-33, esp. 7:22-23 and Figure 3C; 7:39-45 and Figures. 4A-4D; 7:46-52, esp. 7:49-50 and Fig. 4A; claim 23.</p> <p>Included is the intrinsic support for disputed term “disposed in a second position.”</p>	<p>in an orientation where the first projection is located near an upper edge of the frame</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 2:1-8; 2:66-3:19; 5:36-6:3; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 1/25/06 Office Action, pages 8-9; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>
first position	A	<p>See above construction for "disposed in a first position."</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term “disposed in a first position.”</p>	(see above)

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT Q
AU OPTRONICS USP 7,125,157

Claim Terms	Des.	AUO Construction	LGD Construction
the first supporting portion partially contacts an inner wall of the first constraining portion for positioning the film	L	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>Figures 2A-2B, 3A-3C, 4A-4D; 5:17-22; 5:55-6:3; 6:55-61; 7:22-33; 7:46-8:2.</p>	<p>the first projection touches a top portion of the first passage to support the film and has a gap below the first projection</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 2:1-8; 2:66-3:19; 5:17-22; 5:36-6:3; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 1/25/06 Office Action, pages 8-9; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>
does not contact	L	<p>Plain meaning</p>	<p>does not touch</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 2:1-8; 2:66-3:19; 5:36-6:3; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 1/25/06 Office Action, pages 8-9; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT Q
AU OPTRONICS USP 7,125,157

Claim Terms	Des.	AUO Construction	LGD Construction
disposed in a second position	L	<p>a second position of a liquid crystal display unit where the position is determined by reference to the angle of rotation between the first position and the second position.</p> <p><u>Intrinsic Support</u></p> <p>2:12-26, esp. 2:19-25; 2:52-60; 3:6-11; 4:37-42; 4:48-56, esp. Figure 3B; 5:55-6:3, esp. 5:55-57 and Figure 3B; 7:22-33, esp. 7:22-23, 7:26-27, and Figure 3C; 7:39-45 and Figures. 4A- 4D; 7:53-59, esp. 7:55-57 and Figure 4B; claim 23.</p> <p>Included is the intrinsic support for disputed term “disposed in a first position.”</p>	<p>in an orientation rotated from the first position so that the second projection is located near an upper edge of the frame</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 2:1-8; 2:66-3:19; 5:36-6:3; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 1/25/06 Office Action, pages 8-9; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>
second position	A	<p>See above construction for "disposed in a second position."</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term “disposed in a second position.”</p>	(see above)

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT Q
AU OPTRONICS USP 7,125,157

Claim Terms	Des.	AUO Construction	LGD Construction
the second supporting portion partially contacts an inner wall of the second constraining portion for positioning the film	L	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>Figures 2A-2B, 3A-3C, 4A-4D; 5:17-22; 5:55-6:3; 6:55-61; 7:22-33; 7:46-8:2.</p>	<p>the second projection touches a top portion of the second passage to support the film and has a gap below the second projection</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 2:1-8; 2:66-3:19; 5:17-22; 5:36-6:3; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 1/25/06 Office Action, pages 8-9; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>
on opposite corners of the film	L	<p>Plain meaning</p>	<p>through areas where two edges of the film intersect such that the areas do not share an edge of the film</p> <p><u>Intrinsic Support</u></p> <p>2:47-9; 7:34-9; Fig. 3C.</p>
on adjacent corners of the film	L	<p>Plain meaning</p>	<p>through areas where two edges of the film intersect such that the areas share one edge of the film</p> <p><u>Intrinsic Support</u></p> <p>2:47-9; 6:15-22; Fig. 3C.</p>

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AU OPTRONICS USP 7,125,157

Claim Terms	Des.	AUO Construction	LGD Construction
frame comprising a first supporting portion and a second supporting portion	L	See above constructions for "a first supporting portion, disposed on the frame" and "a second supporting portion, further disposed on the frame." <u>Intrinsic Support</u> Same as for the term "supporting portion."	(see constructions above)
a third constraining portion and a fourth constraining portion disposed on the frame		Plain meaning	Indefinite
the third constraining portion and the fourth constraining portion pass through the first constraining portion and the second constraining portion, respectively		Plain meaning	Indefinite

EXHIBIT R

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT R
CHI MEI USP 5,619,352

Disputed Constructions

Claim Terms	Des.	CMO Construction	LGD Construction
a layer of a birefringent material	L	<p>a layer of material that has varying indices of refraction depending on the direction light travels through the material. An index of refraction is the ratio of the speed of light in a medium relative to the speed of light in a vacuum</p> <p><u>Intrinsic Support</u></p> <p>2:53-3:14; 10:27-11:8; 12:23-38; 16:1-17:35; 17:59-20:51; Fig. 14</p>	<p>a thickness of material including positively birefringent molecules that are uniaxial or near uniaxial in character</p> <p><u>Intrinsic Support</u></p> <p>2:53-3:19; 7:08-22; 8:16-53; 9:37-10:47; 10:51-64; 12:45-50; 13:08-20; 14:48-57; 15:63-67; 16:03-10; Figs. 7-14; Abstract; App 08/223,251, 8/23,1995, Amendment, pages 6-9.</p>
optical symmetry axis	L	<p>the extraordinary optic axis in uniaxial materials and the principal optic axis in biaxial materials. A uniaxial material has two axes with the same index of refraction and another axis, the extraordinary axis, that has a different index of refraction. A biaxial material has three axes each with a different index of refraction, and the axis with the highest index of refraction is the principal optic axis</p> <p><u>Intrinsic Support</u></p> <p>2:61-3:17; 10:27-11:8; 12:23-38; 16:1-17:35; 17:59-20:51; Fig. 14</p>	<p>the extraordinary axis of the molecules</p> <p>or</p> <p>Indefinite</p> <p><u>Intrinsic Support</u></p> <p>2:53-3:19; 9:37-10:47; 10:51-64.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT R
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Claim Terms	Des.	CMO Construction	LGD Construction
tilt angle varies along an axis normal to said layer	L	<p>the tilt angle at a bottom surface of the layer is different than the tilt angle at a top surface of the layer relative to an axis normal (perpendicular) to the layer</p> <p><u>Intrinsic Support</u></p> <p>3:50-61; 11:13-17; 12:42-54; 17:59-20:51; Fig. 2; Fig. 12; Application 08/313,476, Response, January 22, 1996</p>	<p>the tilt angle of the compensator varies along an axis normal to the layer of birefringent material and is limited to values between approximately 25 degrees and approximately 65 degrees</p> <p><u>Intrinsic Support</u></p> <p>7:08-22; 10:65-11:21; 12:23-26; 14:04-07; 14:33-44; 16:16-19; Figs. 7-14; Title & Abstract; App 08/223,251, 8/23,1995, Amendment, pages 6-9 ; App 08/690,033, 1/22/1996, Amendment, pages 9-11.</p>
a desired viewing characteristic over a specified field of view		<p>A contrast ratio that exceeds a threshold for a specified range of viewing angles. The contrast ratio is a luminance at a bright state divided by a luminance at a dark state.</p> <p><u>Intrinsic Support</u></p> <p>1:57-2:21; 5:1-8:42; 10:17-25; 10:49-59; 17:59-20:51; Fig. 4; Fig. 5; Fig. 6; Fig. 7; Fig. 8; Fig. 9; Fig. 10</p>	Indefinite

EXHIBIT S

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT S
CHI MEI USP 6,008,786

Disputed Constructions

Claim Terms	Des.	CMO Construction	LGD Construction
driver means	L	<p>Function (plain meaning): driving the display cell with grey scale data signals</p> <p>Corresponding structure: X-driver 3, Y-driver 5 (Fig. 1) and equivalents</p> <p><u>Intrinsic Support</u></p> <p>1:27-46; 1:47-52; 6:1-9; and exhibits referenced therein, including Fig. 1</p>	<p>Interpreted per 35 USC §112¶6</p> <p>function: driving the display cell with sets of grey scale data signals</p> <p>structure: Fig. 1, element 3</p> <p><u>Intrinsic Support</u></p> <p>1:27-46; 2:46-3:11; 3:64-4:06; Fig. 1.</p>
data control means	L	<p>Function (plain meaning): receiving gray scale data signals and outputting the gray scale data signals to the driver with a predetermined timing</p> <p>Corresponding structure: computing circuit 32, buffer circuit 26, delay circuit 24 (Fig. 5) and equivalents</p> <p><u>Intrinsic Support</u></p> <p>4:31-37; 5:23-30; 3:25-31; 5:58-63; 6:1-9; and exhibits referenced therein, including Fig. 5</p>	<p>Interpreted per 35 USC §112¶6</p> <p>function: receiving gray scale data signals related to the setting of a gray scale for the display cell and outputting said gray scale data signals to said driver with a predetermined timing</p> <p>structure: Fig. 5, all elements; Figs 6-8</p> <p><u>Intrinsic Support</u></p> <p>1:27-46; 1:66-2:27; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 5:11-43; 5:58-63; Figs. 1, 2, 5, 6, 7.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT S
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Claim Terms	Des.	CMO Construction	LGD Construction
computing means	L	<p>Function (plain meaning): changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium</p> <p>Corresponding structure: computing circuit 32 (Fig. 5) and equivalents</p> <p><u>Intrinsic Support</u></p> <p>4:31-37; 5:58-63; 2:1-23; 3:25-31; 4:55-57; 6:1-9; and exhibits referenced therein, including Fig. 5</p>	<p>Interpreted per 35 USC §112¶6</p> <p>function: changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium</p> <p>structure: Fig. 5, elements 32, 33, 34; Figs. 6-8</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 4:55-5:10; 5:11-43; 5:58-63; Figs. 5, 6, 7, 8.</p>
changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level	L	<p>see claim 1 “computing means” above</p>	<p>adding or subtracting compensation values to modify the gray scale levels of one or more, but not all, color video signals</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:27-46; 1:66-2:27; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 4:55-5:10; 5:11-43; 5:58-63; Figs. 1, 2, 5, 6, 7, 8; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT S
CHI MEI USP 6,008,786

Claim Terms	Des.	CMO Construction	LGD Construction
buffer means	L	<p>plain meaning</p> <p>or, if the Court determines construction is necessary,</p> <p>memory where gray scale data signals can be temporarily stored and delayed</p> <p>if interpreted pursuant to 35 U.S.C. §112, ¶6:</p> <p>Function (plain meaning): delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected</p> <p>Corresponding structure: buffer circuit 26, delay circuit 24 (Fig. 5) and equivalents</p> <p><u>Intrinsic Support</u></p> <p>5:23-30; 4:11-21; 6:1-9; and exhibits referenced therein, including Fig. 5</p>	<p>Interpreted per 35 USC §112¶6</p> <p>function: delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected</p> <p>structure: Fig. 5, element 24</p> <p>Indefinite</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:46-3:11; 3:12-32; 3:64-4:06; 5:11-43; 4:07-56; Figs. 5, 6, 7.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT S
CHI MEI USP 6,008,786

Claim Terms	Des.	CMO Construction	LGD Construction
delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected	L	see claim 1 "buffer means" above	holding or deferring at least one color video signal that is not subjected to a compensation value by the amount of time taken to modify another color video signal <u>Intrinsic Support</u> Abstract; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 5:11-43; Figs. 5, 6, 7; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.
adjusting means	L	Function (plain meaning): varying the amount of correction accorded to the gray scale data signals for said at least one color Corresponding structure: computing circuit 32 (Fig. 5) and equivalents <u>Intrinsic Support</u> 5:37-43; 4:31-37; 3:25-31; 5:56-63; 6:1-9; and exhibits referenced therein, including Fig. 5	Interpreted per 35 USC §112¶6 function: varying the amount of correction accorded to the gray scale data signals for said at least one color structure: Fig. 5, elements 33, 34; Figs. 6-8 <u>Intrinsic Support</u> 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 4:55-5:10; 5:11-43; 5:58-63; Figs. 5, 6, 7, 8.

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT S
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Claim Terms	Des.	CMO Construction	LGD Construction
said adjusting means (claim 3)		<p>Function (plain meaning): delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected</p> <p>Corresponding structure: buffer circuit 26, delay circuit 24 (Fig. 5) and equivalents</p> <p><u>Intrinsic Support</u></p> <p>5:23-30; 4:11-21; 6:1-9; and exhibits referenced therein, including Fig. 5</p>	Indefinite
changing the level of gray scale data signals related to at least one of the multicolors supplied to the display cell to create a corrected gray scale data signal with a level different from the inputted gray scale data signal	L	<p>plain meaning</p> <p>or, if the Court determines construction is necessary,</p> <p>changing the level of gray scale data signals related to at least one of the multicolors supplied to the display cell to create a corrected gray scale data signal</p> <p><u>Intrinsic Support</u></p> <p>4:31-37; 5:58-63; 2:1-23; 3:25-31; 4:55-57; 6:1-9; and exhibits referenced therein</p>	<p>adding or subtracting compensation values to modify the gray scale levels of one or more, but not all, input color video signals</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:27-46; 1:66-2:27; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 4:55-5:10; 5:11-43; 5:58-63; Figs. 1, 2, 5, 6, 7, 8; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>

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Claim Terms	Des.	CMO Construction	LGD Construction
delaying the output for at least one other of the multicolor by the time taken for correction of said at least one color	L	<p>plain meaning</p> <p>or, if the Court determines construction is necessary,</p> <p>delaying the output for at least one other of the multicolors by the time taken for correction of said at least one color</p> <p><u>Intrinsic Support</u></p> <p>5:23-30; 4:11-21; 6:1-9; and exhibits referenced therein</p>	<p>holding or deferring the output of at least one color video signal that is not subject to a compensation value by the amount of time taken to modify another color video signal</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 5:11-43; Figs. 5, 6, 7; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>

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Claim Terms	Des.	CMO Construction	LGD Construction
simultaneously output the gray scale data of all said multicolors	L	<p>plain meaning</p> <p>or, if the Court determines construction is necessary,</p> <p>outputting the gray scale data of all the multicolors from a buffer at about the same time</p> <p><u>Intrinsic Support</u></p> <p>3:29-31; 4:19-21; 5:23-30; 4:11-18; 6:1-9; and exhibits referenced therein</p>	<p>provides all multicolor gray scale data to the data driver during the same predetermined time interval</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:27-46; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 5:11-43; Figs. 1, 5, 6, 7; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>
display cells		plain meaning	Indefinite

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT S
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Claim Terms	Des.	CMO Construction	LGD Construction
calculation logic . . . for changing the level of the gray scale data signals of said at least one color to a different gray scale level	L	<p>plain meaning</p> <p>or, if the Court determines construction is necessary,</p> <p>structure, including a driver circuit, that changes the gray scale data signal for at least one color relative to the other colors</p> <p><u>Intrinsic Support</u></p> <p>4:31-37; 5:58-63; 2:1-23; 3:25-31; 4:55-57; 6:1-9; and exhibits referenced therein</p>	<p>calculation logic . . . for adding or subtracting compensation values to modify one or more, but not all, color video signals</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:27-46; 1:66-2:27; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 4:55-5:10; 5:11-43; 5:58-63; Figs. 1, 2, 5, 6, 7, 8; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>
driver circuit for any other of the colors without the calculation logic in its driver circuit	L	<p>plain meaning</p> <p>see claim 7 “calculation logic” above.</p>	<p>at least one color video signal path that does not include calculation logic</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 5:11-43; Figs. 5, 6, 7; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>

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Claim Terms	Des.	CMO Construction	LGD Construction
delaying the gray scale signals for the other of the colors	L	<p>plain meaning</p> <p>see claim 5 “delaying the output for at least one other of the multicolor by the time taken for correction of said at least one color” above</p>	<p>holding or deferring the output of the unmodified color video signals</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 5:11-43; Figs. 5, 6, 7; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>
said data control means (claim 11)		<p>structure that can add or subtract a binary signal representing a change of at least one gray scale level for at least one color</p> <p>see also claim 7, “calculation logic” below</p> <p><u>Intrinsic Support</u></p> <p>3:25-31; 4:31-37; 5:58-63; 2:1-23; 4:55-57; 6:1-9; and exhibits referenced therein, including Fig. 5</p>	Indefinite

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Claim Terms	Des.	CMO Construction	LGD Construction
changing the gray scale data signals related to one of the multicolors	L	<p>plain meaning</p> <p>or, if the Court determines construction is necessary,</p> <p>changing the gray scale data signals for at least one of the multicolors</p> <p><u>Intrinsic Support</u></p> <p>4:31-37; 5:58-63; 2:1-23; 3:25-31; 4:55-57; 6:1-9; and exhibits referenced therein</p>	<p>adding or subtracting compensation values to modify the gray scale level of one of the color video signals</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:27-46; 1:66-2:27; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 4:55-5:10; 5:11-43; 5:58-63; Figs. 1, 2, 5, 6, 7, 8; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>

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Claim Terms	Des.	CMO Construction	LGD Construction
delaying the output for any other color of the multicolors with gray scale data signals not subject to a correction by the amount of time taken for correction of the one color	L	<p>plain meaning</p> <p>or, if the Court determines construction is necessary,</p> <p>delaying the output for any uncorrected color of the multicolors by the amount of time taken for correction of the one color</p> <p><u>Intrinsic Support</u></p> <p>5:23-30; 4:11-21; 6:1-9; and exhibits referenced therein</p>	<p>holding or deferring the output of the remaining color video signals that are not subject to compensation values by the amount of time taken to modify the one color video signal</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 5:11-43; Figs. 5, 6, 7; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>
synchronize the timing of the gray scale data signals for all said multicolors	L	<p>plain meaning</p> <p>see also claim 5 “simultaneously output the gray scale data of all said multicolors” above</p>	<p>provides all multicolor gray scale data signals to the data driver during the same predetermined time interval</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:27-46; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 5:11-43; Figs. 1, 5, 6, 7; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>

EXHIBIT T

JOINT CLAIM CONSTRUCTION STATEMENT EXHIBIT T
CHI MEI USP 6,013,923

Disputed Constructions

Claim Terms	Des.	CMO Construction	LGD Construction
source line	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>conductor that connects the source terminals of pixel transistors and leads to the source amplifiers</p> <p><u>Intrinsic Support</u></p> <p>4:65-66; 5:1-5:6; 7:22-31; 7:66-8:2 and exhibits referenced therein</p>	<p>a pattern of electrically conductive material that conveys data signals to transistors within the TFT array</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:6-11; 1:12-2:17; 2:58-65; 3:6-31, 3:39-43; 3:45-4:31; 4:64-5:15; 5:27-41; 5:48-6:19; 7:1-31; 7:49-8:2; Figs. 1-3, 6-8.</p>
gate line	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>conductor that connects the gate terminals of pixel transistors and leads to the gate driver circuit</p> <p><u>Intrinsic Support</u></p> <p>4:64-65; 4:66-5:1; 7:22-31; 7:66-8:2 and exhibits referenced therein</p>	<p>a pattern of electrically conductive material that conveys gate signals to transistors within the TFT array</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:6-11; 1:12-2:17; 2:58-65; 3:6-31, 3:39-43; 3:45-4:31; 4:64-5:15; 5:27-47; 5:65-6:19; 7:1-31; 7:49-8:2; Figs. 1-3, 6-8.</p>

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Claim Terms	Des.	CMO Construction	LGD Construction
during formation of said gate lines	L	<p>during the manufacturing stages in which the gate lines are formed and connected</p> <p><u>Intrinsic Support</u></p> <p>7:22-31; 4:64-5:1; 5:27-40; 7:49-55; 5:41-64; 1:55-62; 7:66-8:2 and exhibits referenced therein</p>	<p>at the same time when the electrically conductive material that forms the gate lines is deposited and etched</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:6-11; 1:12-2:17; 2:58-65; 3:6-31, 3:39-43; 3:45-4:31; 4:64-5:15; 5:27-47; 5:65-6:19; 7:1-31; 7:49-8:2; Figs. 3-9; App. No. 09/000,479, 11/3/1997, PCT International Preliminary Examination Report, pages 2-4.</p>
shorting element	L	<p>plain meaning</p> <p><u>Intrinsic Support</u></p> <p>see, e.g., 1:64-2:3 and exhibits referenced therein</p>	<p>a pattern of conductive material for electrically connecting, with low resistance, the gate lines to each other or the source lines to each other</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:55-2:3; 1:7-10; 1:12-20; 1:24-27; 1:44-2:10; 2:19-28; 2:44-51; 2:58-68; 3:6-30; 3:54-62; 4:5-31; 5:38-64; 6:14-35; 6:47-57; 7:1-21; 7:36-40; 7:49-8:2; Figs. 3-9; App. No. 09/000,479, 11/3/1997, PCT International Preliminary Examination Report, pages 2-4.</p>

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Claim Terms	Des.	CMO Construction	LGD Construction
protection element	L	<p>element protecting from electrostatic discharge (ESD)</p> <p><u>Intrinsic Support</u></p> <p>5:60-6:13; 4:24-26; 2:61-67; 7:66-8:2 and exhibits referenced therein</p>	<p>a circuit component designed to protect against electrostatic discharge and to allow for testing</p> <p><u>Intrinsic Support</u></p> <p>1:5-10; 1:12-20; 1:24-26; 1:31-43; 1:55-3:43; 3:45-50; 3: 54-61; 4:5-22; 4:27-32; 5:33-41; 5:50-6:13; 6:19-57; 7:15-40; 7:49-8:2; Figs. 3-9; App. No. 09/000,479, 11/3/1997, PCT International Preliminary Examination Report, pages 2-4.</p>
during formation of said source lines	L	<p>during the manufacturing stages in which the source lines are formed and connected</p> <p><u>Intrinsic Support</u></p> <p>7:22-31; 5:1-5:6; 7:49-55; 5:30-34; 5:48-57; 1:55-62; 7:66-8:2 and exhibits referenced therein</p>	<p>at the same time when the electrically conductive material that forms the source lines is deposited and etched</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:6-11; 1:12-2:17; 2:58-65; 3:6-31, 3:39-43; 3:45-4:31; 4:64-5:15; 5:27-41; 5:48-6:19; 7:1-31; 7:49-8:2; Figs. 3-9; App. No. 09/000,479, 11/3/1997, PCT International Preliminary Examination Report, pages 2-4.</p>

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Claim Terms	Des.	CMO Construction	LGD Construction
electrically coupling said shorting elements	L	<p>electrically connecting the shorting elements</p> <p><u>Intrinsic Support</u></p> <p>5:57-64; 7:66-8:2 and exhibits referenced therein</p>	<p>electrically connecting the shorting elements without intervening protection elements</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:55-2:3; 1:7-10; 1:12-20; 1:24-27; 1:44-2:10; 2:19-28; 2:44-51; 2:58-68; 3:6-30; 3:54-62; 4:5-31; 5:7-14; 5:38-64; 6:14-35; 6:47-57; 7:1-21; 7:36-40; 7:49-8:2; Figs. 3-9; App. No. 09/000,479, 11/3/1997, PCT International Preliminary Examination Report, pages 2-4.</p>

EXHIBIT U

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT U
CHI MEI USP 6,134,092

Disputed Constructions

Claim Terms	Des.	CMO Construction	LGD Construction
peripheral portion	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>a portion of the waveguide that is covered by a cover</p> <p><u>Intrinsic Support</u></p> <p>5:9-14; 6:66-7:2; 7:12-15; 9:30-12:9; Fig. 12; Fig. 13</p>	<p>boundary adjacent a side edge</p> <p><u>Intrinsic Support</u></p> <p>1:43-52, 66-67; 3:18-22; 5:9-15; 7:3-15; 7:26-30; 7:55-59; Figs. 5, 6A, 13, 13A.</p>
a series of point light sources	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>three or more solid state light sources</p> <p><u>Intrinsic Support</u></p> <p>1:24-34; 1:54-56; 3:18-22; 7:3-5; 9:30-12:9</p>	<p>a sequence of separate components, such as light-emitting diodes, that provide the desired light that illuminates the waveguide or optical cavity</p> <p><u>Intrinsic Support</u></p> <p>1:61-5; 2:5-9; 3:15-30; 6:45-50; 7:27-31; Figs. 2, 11, 13, and 13A; App 09/057,199, 3/23/00 Notice of Allowability, pages 2-4.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT U
CHI MEI USP 6,134,092

Claim Terms	Des.	CMO Construction	LGD Construction
diffusive reflective surfaces	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>surfaces, including a surface that extends upward relative to a planar surface, that diffusively reflect light</p> <p><u>Intrinsic Support</u></p> <p>3:44-47; 4:24-54; 5:61-6:7; 7:16-26; 7:44-61; 9:30-12:9; Fig. 2; Fig. 4; Fig. 8; Fig. 13; Fig. 13A</p>	<p>non-transparent boundaries of an object that reflect and scatter light from the point light source</p> <p><u>Intrinsic Support</u></p> <p>1:44-52; 2:10-6; 3:42-4:3; 4:24-54; 6:1-7; 6:44-61; 7:3-15; Figs. 3, 11, 13, 13A; App 09/057,199, 3/23/00 Notice of Allowability, pages 2-4.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT U
CHI MEI USP 6,134,092

Claim Terms	Des.	CMO Construction	LGD Construction
oriented relative to the series of point light sources and the waveguide so as to introduce light	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>construe:</p> <p>“the diffusive reflective surfaces oriented relative to the series of point light sources and the waveguide so as to introduce light in regions of said waveguide between pairs of said point light sources”</p> <p>to mean:</p> <p>the diffusive reflective surfaces are angled relative to each other to direct light from the point light sources into the waveguide</p> <p><u>Intrinsic Support</u></p> <p>3:54-57; 3:65-4:3; 7:16-23; 7:44-61; 9:30-12:9; Fig. 2; Fig. 3; Fig. 13; Fig. 13A</p>	<p>arranged to be substantially perpendicular to the top surface of the waveguide so as to introduce scattered light reflected directly from the point light sources into the waveguide</p> <p><u>Intrinsic Support</u></p> <p>1:43-52; 3:15-22, 42-4:3; 5:9-15; 7:3-31, 55-9; Figs. 11, 13, 13A.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT U
CHI MEI USP 6,134,092

Claim Terms	Des.	CMO Construction	LGD Construction
whereby the peripheral portion of the waveguide is substantially uniformly illuminated	L C	<p>not a claim limitation</p> <p>or</p> <p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>The portion of the waveguide, that is covered by a cover and intersects an aperture, is substantially uniformly illuminated. The aperture is an area of the waveguide through which light escapes the illumination device.</p> <p><u>Intrinsic Support</u></p> <p>1:17-23; 5:49-54; 5:9-14; 6:66-7:2; 7:12-15; 7:36-39; 9:30-12:9; Fig. 12; Fig. 13</p>	<p>such that the same or nearly the same amount of light is provided along a boundary adjacent a side edge of the waveguide</p> <p><u>Intrinsic Support</u></p> <p>1:47-52; 2:11-17; 3:15-20, 5:1-8; 7:3-15; 7:55-59.</p>
light-emitting diodes mounted on an electrical-conductive strip of material	L	<p>plain meaning</p>	<p>components, each containing a semiconductor diode chip as part of their structure, that provide the desired light that illuminates the waveguide or optical cavity and that are attached to a strip of material that provides electrical signals to the components</p> <p><u>Intrinsic Support</u></p> <p>3:15-31; 6:45-54; Figs. 2, 13, and 13A.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT U
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Claim Terms	Des.	CMO Construction	LGD Construction
mouth	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>construe:</p> <p>“entry mouth”</p> <p>to mean:</p> <p>a region of the optical cavity that is located nearest to the point light source</p> <p>and construe:</p> <p>“exit mouth”</p> <p>to mean:</p> <p>a region of the optical cavity that is located the farthest from the point light source</p> <p><u>Intrinsic Support</u></p> <p>4:10-23; 7:16-30; 9:30-12:9; Fig. 3; Fig. 13</p>	<p>an optical opening through which light passes</p> <p><u>Intrinsic Support</u></p> <p>4:10-23; 6:48-9; Figs. 2, 3, 10, 13 and 13A.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT U
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Claim Terms	Des.	CMO Construction	LGD Construction
diffusive reflective optical cavities	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>a space between diffusive reflective surfaces</p> <p><u>Intrinsic Support</u></p> <p>3:44-47; 4:24-54; 5:61-6:7; 7:5-12; 7:16-26; 7:44-61; 9:30-12:9; Fig. 2; Fig. 8; Fig. 11; Fig. 12; Fig. 13; Fig. 13A</p>	<p>optical passages having non-transparent surfaces that reflect and scatter light from the point light source</p> <p><u>Intrinsic Support</u></p> <p>1:61-65; 2:1-9; 4:10-23; 7:3-15; 7:44-61; Fig. 13A.</p>
guide members positioned along a periphery of the optical cavity	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>guide members are spaced apart along a side of the optical cavity</p> <p><u>Intrinsic Support</u></p> <p>3:42-44; 9:30-12:9; Fig. 2; Fig. 3; Fig. 11; Fig 13; Fig. 13A</p>	<p>separate structures, unattached from one another, each adjacent a side edge of the optical cavity</p> <p><u>Intrinsic Support</u></p> <p>3:15-20; 3:42-67; 4:10-24; 7:3-31; 7:50-60; Figs. 3, 4, 11, 13.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT U
CHI MEI USP 6,134,092

Claim Terms	Des.	CMO Construction	LGD Construction
whereby light is injected from said exit mouths into a peripheral portion of said optical cavity	C	<p>not a claim limitation</p> <p>or</p> <p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>light is injected from regions of the optical cavities farthest from the point sources of light into a portion of the optical cavity that is covered by a cover</p> <p><u>Intrinsic Support</u></p> <p>3:18-22; 5:9-14; 6:66-7:26; 9:30-12:9; Fig. 3; Fig. 11; Fig. 12; Fig. 13; Fig. 13A</p>	<p>such that light is injected from said exit mouths into a boundary adjacent a side edge of the optical cavity</p> <p><u>Intrinsic Support</u></p> <p>1:43-52, 66-7; 3:18-22; 4:10-23; 5:9-15; 7:3-31, 26-30, 55-9; Figs. 5, 6A, 13, 13A.</p>

EXHIBIT V

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT V
CHI MEI USP 6,734,926

Disputed Constructions

Claim Terms	Des.	CMO Construction	LGD Construction
display apparatus	L	<p>plain meaning</p> <p><u>Intrinsic Support</u></p> <p>Abstract, 1:7-11, 36-39, 2:17-3:24, 3:63-4:12, 4:50-5:21, 5:37-6:14, 6:28-50, 6:65-7:16, 7:24-33, 7:52-8:3, 8:28-33, Figs. 4-13</p>	<p>a display product, such as a monitor or television</p> <p><u>Intrinsic Support</u></p> <p>1:8-11, 36-53; 2:1-11; 8:4-27; Figs. 1, 3-13.</p>
upper frame	L	<p>plain meaning</p> <p><u>Intrinsic Support</u></p> <p>1:39-44, 2:17-24, 33-35, 51-54, 2:66-3:2, 4:1-3, 50-51, 5:1-3, 37-38, 55-58, 6:31-34, 8:28-33, Figs. 1, 4-13</p>	<p>the outermost front cover for the display product</p> <p><u>Intrinsic Support</u></p> <p>1:8-11, 36-53; 2:1-11; 8:4-27; Figs. 1, 3-13.</p>
an array of light tubes disposed behind the display panel	L	<p>plain meaning</p> <p><u>Intrinsic Support</u></p> <p>Abstract, 1:10-11, 45-53, 2:1-11, 17-22, 33-37, 51-55, 2:66-3:4, 4:1-5, 50-51, 5:1-5, 37-38, 55-59, 6:31-35, 8:28-33, Figs. 1, 4-13</p>	<p>multiple fluorescent lamps arranged along the back of the direct type backlight unit</p> <p><u>Intrinsic Support</u></p> <p>2:1-11; 3:18-24; 8:4-16; Figs. 4-13.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT V
CHI MEI USP 6,734,926

Claim Terms	Des.	CMO Construction	LGD Construction
being separated from the side portion by a gap	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>there is a space between one side of a subframe of the supporting frame and the side portion of the reflecting plate</p> <p><u>Intrinsic Support</u></p> <p>2:24-32, 4:7-20, 50-62, 8:28-33, Figs. 4-5</p>	<p>positioned to form a space bounded by a sub-frame and a side portion</p> <p><u>Intrinsic Support</u></p> <p>4:35-39, 54-64; 5:15-21, 30-36, 40-51; 6:6-13, 49-51; 8:4-27; Figs. 4-7.</p>
a circuit board installed within the gap for controlling operations of the display apparatus	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>a rigid or printed circuit board for controlling certain operations of the display apparatus located in the space defined above</p> <p><u>Intrinsic Support</u></p> <p>2:24-32, 2:44-50, 4:7-20, 4:32-39, 50-62, 5:7-22, 30-33, 37-38, 41-51, 8:28-33, Figs. 4-7</p>	<p>a control circuit board is mounted in the space bounded by the sub-frame and the side portion and no control circuit board is located on the back of the supporting plate or reflecting plate</p> <p><u>Intrinsic Support</u></p> <p>1:7-11; 1:54-2:7; 3:18-24, 61-63; 5:19-21, 30-36; 6:25-27, 62-64; 8:4-27; Figs. 4-13; App 10/065,039, 1/26/01 Notice of Allowability, page 2.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT V
CHI MEI USP 6,734,926

Claim Terms	Des.	CMO Construction	LGD Construction
being separated from the side portion of the supporting plate by a gap	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>there is a space between one side of a subframe of the supporting frame and the side portion of the supporting plate</p> <p><u>Intrinsic Support</u></p> <p>2:44-50, 5:7-20, 37-38, 41-51, 8:28-33, Figs. 6-7</p>	<p>positioned to form a space bounded by a sub-frame and a side portion</p> <p><u>Intrinsic Support</u></p> <p>4:35-39, 54-64; 5:15-21, 30-34; 5:40-51; 6:6-13, 49-51; 8:4-27; Figs. 4-7.</p>
a circuit board installed on the side portion of the reflecting plate for controlling operations of the display apparatus	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>a rigid or printed circuit board for controlling certain operations of the display apparatus mechanically supported by the side portion of the reflecting plate</p> <p><u>Intrinsic Support</u></p> <p>2:58-65, 5:62-6:23, 8:28-33, Figs. 8-9</p>	<p>a control circuit board is mounted to the side of the reflecting plate and no control circuit board is located on the back of the supporting plate or reflecting plate</p> <p><u>Intrinsic Support</u></p> <p>1:7-11; 1:54-2:7; 3:18-24, 61-63; 6:25-27, 62-64; 8:4-27; Figs. 4-13; App 10/065,039, 1/26/01 Notice of Allowability, page 2.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT V
CHI MEI USP 6,734,926

Claim Terms	Des.	CMO Construction	LGD Construction
a circuit board installed on the side portion of the supporting plate for controlling operations of the display apparatus	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>a rigid or printed circuit board for controlling certain operations of the display apparatus mechanically supported by the side portion of the supporting plate</p> <p><u>Intrinsic Support</u></p> <p>3:3-17, 6:38-62, 8:28-33, Figs. 10-11</p>	<p>a control circuit board is mounted to the side of the supporting plate and no control circuit board is located on the back of the supporting plate or reflecting plate</p> <p><u>Intrinsic Support</u></p> <p>1:7-11; 1:54-2:7; 3:18-24, 61-3; 6:25-27, 62-64; 8:4-27; Figs. 4-13; App 10/065,039, 1/26/01 Notice of Allowability, page 2.</p>
integrated supporting unit	L	<p>a component including a supporting frame portion and either a reflecting plate portion or a supporting plate portion</p> <p><u>Intrinsic Support</u></p> <p>6:67-7:17, 7:27-43, 8:28-33, Figs. 12-13</p>	<p>a unitary structure that provides support</p> <p><u>Intrinsic Support</u></p> <p>4:5-20; 6:65-7:15; 7:26-40; Fig. 4.</p>
a circuit board installed on at least one of the side portions of the reflecting plate for controlling operations of the display apparatus		<p>a rigid or printed circuit board for controlling certain operations of the display apparatus mechanically supported by the side portion of the integrated supporting unit</p> <p><u>Intrinsic Support</u></p> <p>2:58-65, 5:62-6:23, 6:67-7:17, 8:28-33, Figs. 8-9, 12</p>	Indefinite

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT V
CHI MEI USP 6,734,926

Claim Terms	Des.	CMO Construction	LGD Construction
a circuit board installed on at least one of the side portions of the supporting plate for controlling operations of the display apparatus		<p>a rigid or printed circuit board for controlling certain operations of the display apparatus mechanically supported by the side portion of the integrated supporting unit</p> <p><u>Intrinsic Support</u></p> <p>3:3-17, 6:38-62, 7:27-43, 8:28-33, Figs. 10-11</p>	Indefinite

EXHIBIT W

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT W
CHI MEI USP 7,280,179

Disputed Constructions

Claim Terms	Des.	CMO Construction	LGD Construction
forming a sealing member having a main portion enclosing a display region	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>forming sealing material in a closed shape having four side walls for fixing a pair of substrates to each other and sealing the liquid crystal layer in the display region</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:6-11; 1:17-39; 1:49-2:5; 2:17-28; 2:40-67; 3:7-15; 3:20-27; 3:45-54; 3:67-4:31; 4:34-37; 4:65-5:7; Figs. 1-4; App. 10/921,508, 4/26/06 Response, pages 8, 9, 10; 9/25/06 Amendment, pages 9, 10, 11, 12</p>	<p>depositing sealant material parallel to the edges of the display region so that it encloses the display region</p> <p><u>Intrinsic Support</u></p> <p>1:29-32, 49-52; 4:12-31; 5:3-7; Figs. 2, 3, and 4; App 10/921,508, 4/26/06 Response, pages 8-10, 12 and 13; App 10/921,508, 9/26/06 Response, pages 9-17; App 10/921,508, 3/1/07 Response, pages 10-16.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT W
CHI MEI USP 7,280,179

Claim Terms	Des.	CMO Construction	LGD Construction
the sealing member has a main portion enclosing a display region	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>sealing material in a closed shape having four side walls for fixing a pair of substrates to each other and sealing the liquid crystal layer in the display region</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:6-11; 1:17-39; 1:49-2:5; 2:17-28; 2:40-67; 3:7-15; 3:20-27; 3:45-54; 3:67-4:31; 4:34-37; 4:65-5:7; Figs. 1-4; App. 10/921,508, 4/26/06 Response, pages 8, 9, 10; 9/25/06 Amendment, pages 9, 10, 11, 12</p>	<p>the sealing member has a portion of sealant material that is parallel to the edges of and encloses the display region</p> <p><u>Intrinsic Support</u></p> <p>1:29-32, 49-52; 4:12-31; 5:3-7; Figs. 2, 3, and 4; App 10/921,508, 4/26/06 Response, pages 8-10, 12 and 13; App 10/921,508, 9/26/06 Response, pages 9-17; App 10/921,508, 3/1/07 Response, pages 10-16.</p>
overlapping area extends along one side of the display region	L	<p>plain meaning</p> <p><u>Intrinsic Support</u></p> <p>1:52-56; 2:56-67; 3:7-15; 4:18-31; 4:65-5:7; Figs. 1-4</p>	<p>a segment of the sealing member main portion where sealant material is applied on top of previously applied sealant material along one edge of the display region</p> <p><u>Intrinsic Support</u></p> <p>1:52-61; 4:12-31; Figs. 2, 3, and 4; App 10/921,508, 3/1/07 Response, pages 10-16; App 10/921,508, 6/5/07 Reasons for Allowability, page 2.</p>

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT W
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Claim Terms	Des.	CMO Construction	LGD Construction
applying the sealing material along the display region to form the main portion of the sealing member	L	<p>Plain and ordinary meaning in light of previous constructions.</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:6-11; 1:17-39; 1:49-2:5; 2:17-28; 2:40-67; 3:7-15; 3:20-27; 3:45-54; 3:67-4:31; 4:34-37; 4:65-5:7; Figs. 1-4; App. 10/921,508, 4/26/06 Response, pages 8, 9, 10; 9/25/06 Amendment, pages 9, 10, 11, 12</p>	<p>depositing sealant material parallel to the edges of the display region</p> <p><u>Intrinsic Support</u></p> <p>1:29-32, 49-52; 4:1-31; 5:3-7; Figs. 2, 3, and 4; App 10/921,508, 4/26/06 Response, pages 8-10, 12 and 13; App 10/921,508, 9/26/06 Response, pages 9-17; App 10/921,508, 3/1/07 Response, pages 10-16.</p>